PIC18F2515/2610/4515/4610 Rev. B5 Silicon Errata

The PIC18F2515/2610/4515/4610 family Rev. B5 parts you have received conform functionally to the Device Data Sheet (DS39636**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2515/2610/4515/4610 family will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2515/2610/4515/4610 family devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2515	0000 1100 111	0 0111
PIC18F2610	0000 1100 101	0 0111
PIC18F4515	0000 1100 011	0 0111
PIC18F4610	0000 1100 001	0 0111

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2515/2610/4515/4610 family silicon.

1. Module: MSSP

In SPI Slave mode, with slave select enabled (SSPM<3:0> = 0b0100), the minimum time between the falling edge of the $\overline{SS}$ pin and the first SCK edge is greater than specified in parameter 70 in Table 25-16. The updated specification is shown in bold in Table 1.

The minimum time between the $\overline{SS}$ pin low and an SSPBUF write is also 3 TCY. If the falling edge of the $\overline{SS}$ pin occurs greater than 3 TCY before the first SCK edge or loading SSPBUF, the peripheral will function correctly. Also, if SSPBUF is written prior to the $\overline{SS}$ pin going low, the peripheral will function correctly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING, CKE = 0)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ Input	**3 TCY**	—	ns	

2. Module: MSSP

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Enhanced Capture/Compare/ PWM (ECCP)

With the ECCP configured for Half-Bridge PWM mode (CCP1M<3:0> = 0b1110), the output may be corrupted for particular duty cycle selections. Affected duty cycle values are 0 though 3, and every subsequent increment of 4 (i.e., 7, 11, 15, 19, etc.).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

One bit has been added to the BAUDCON register and one bit has been renamed. The added bit is RXDTP and is in the location, BAUDCON<5>. The renamed bit is the TXCKP bit (BAUDCON<4>), which had been named SCKP.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the TX and RX signals to be inverted (polarity reversed).

Register 17-3, on page 194, will be changed as shown on page 3.

Work around

None required.

Date Codes that pertain to this issue:

All engineering and production devices.

REGISTER 17-3: BAUDCON: BAUD RATE CONTROL REGISTER

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is Active

bit 5 **RXDTP**: Receive Data Polarity Select bit
Asynchronous mode:
1 = Receive data (RX) is inverted. Idle state is a low level.
0 = No inversion of receive data (RX). Idle state is a high level.
Synchronous mode:
1 = Data (DT) is inverted. Idle state is a low level.
0 = No inversion of data (DT). Idle state is a high level.

bit 4 **TXCKP**: Transmit/Clock Polarity Select bit
Asynchronous mode:
1 = Transmit data (TX) is inverted. Idle state is a low level.
0 = No inversion of transmit data (TX). Idle state is a high level.
Synchronous mode:
1 = Idle state for clock (CK) is a high level
0 = Idle state for clock (CK) is a low level

bit 3 **BRG16:** 16-bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode); SPBRGH value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RX pin with the interrupt generated on the falling edge; bit cleared in hardware on following rising edge
0 = RX pin is not monitored or rising edge detected
Synchronous mode:
Unused in this mode.

bit 0 **ABDEN**: Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
0 = Baud rate measurement disabled or completed
Synchronous mode:
Unused in this mode.

5. Module: Master Synchronous Serial Port (MSSP)

When configured for I²C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

In rare situations, when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTA<7> = 0)
- The EUSART is re-enabled (RCSTA<7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2 TCY delay after re-enabling the EUSART.

1. Disable Receive Interrupts (RCIE bit, PIE1<5> = 0).
2. Disable the EUSART (RCSTA<7> = 0).
3. Re-enable the EUSART (RCSTA<7> = 1).
4. Re-enable Receive Interrupts (PIE1<5> = 1).

   (This is the first TCY delay.)
5. Execute a NOP instruction.

   (This is the second TCY delay.)

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (10/2008)

Initial release of this errata. Includes silicon issues 1-2 (MSSP), 3 (Enhanced Capture/Compare/PWM – ECCP), 4 (Enhanced Universal Synchronous Receiver Transmitter – EUSART), 5 (Master Synchronous Serial Port – MSSP) and 6 (Enhanced Universal Synchronous Receiver Transmitter – EUSART).

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