

Product Overview

MPC561

*THE MPC500
FAMILY OF 32-BIT
EMBEDDED
CONTROLLERS*



MPC561

**LOW COST WITHOUT
SACRIFICING
PERFORMANCE**

The MPC561 32-bit embedded microcontroller from Motorola is a cost-effective choice for applications using external memories, thus not requiring functionality from on-chip integrated FLASH. That does not mean that you sacrifice performance.

The MPC561 with its 32-bit RISC core is designed to provide the improved performance, increased flexibility and additional bandwidth necessary for executing complex automotive applications such as powertrain control and suspension control, as well as general applications such as robotics and avionics control.

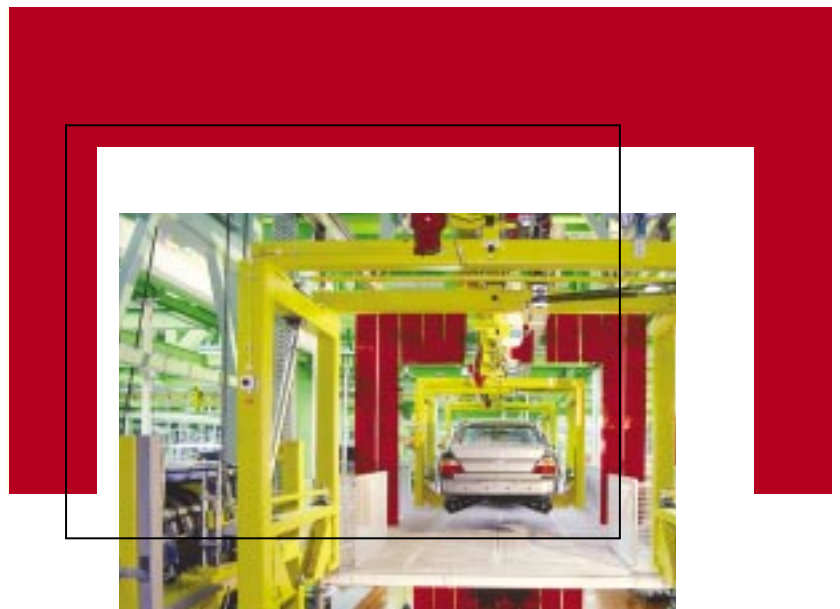
PERFORMANCE FLEXIBILITY

The MPC561 is an ideal solution if you require different memory configuration off- or on-chip. The MPC561 offers 32K bytes of on-chip data RAM. The MPC561 is engineered to

support a more powerful on-board peripheral set than the MPC555, including dual, third generation Time Processing Units (TPU3), each with its own 32-bit RISC engine capable of processing 20 million instructions per second, and three TouCAN™ (CAN 2.0B) controller modules for networking.

Capable of operating in harsh environments at clock speeds of 56 MHz, the MPC561 offers an improved System Integration Unit (SIU) with an enhanced interrupt architecture, a branch target buffer and external burst support to help maximize performance from external memory. The SIU contains a chip select system with address decode designed to support external memories without the need for external GLUE logic.

The MPC561 also offers an enhanced analog to digital converter designed to permit sharing of clocks for synchronous operations.



Code compression is available on the MPC562, helping you save up to 50% in memory space with compact code, freeing up memory to power the computing intense instructions. Compressed code also enables you to load more instructions in the same amount of time, thereby improving CPU performance.

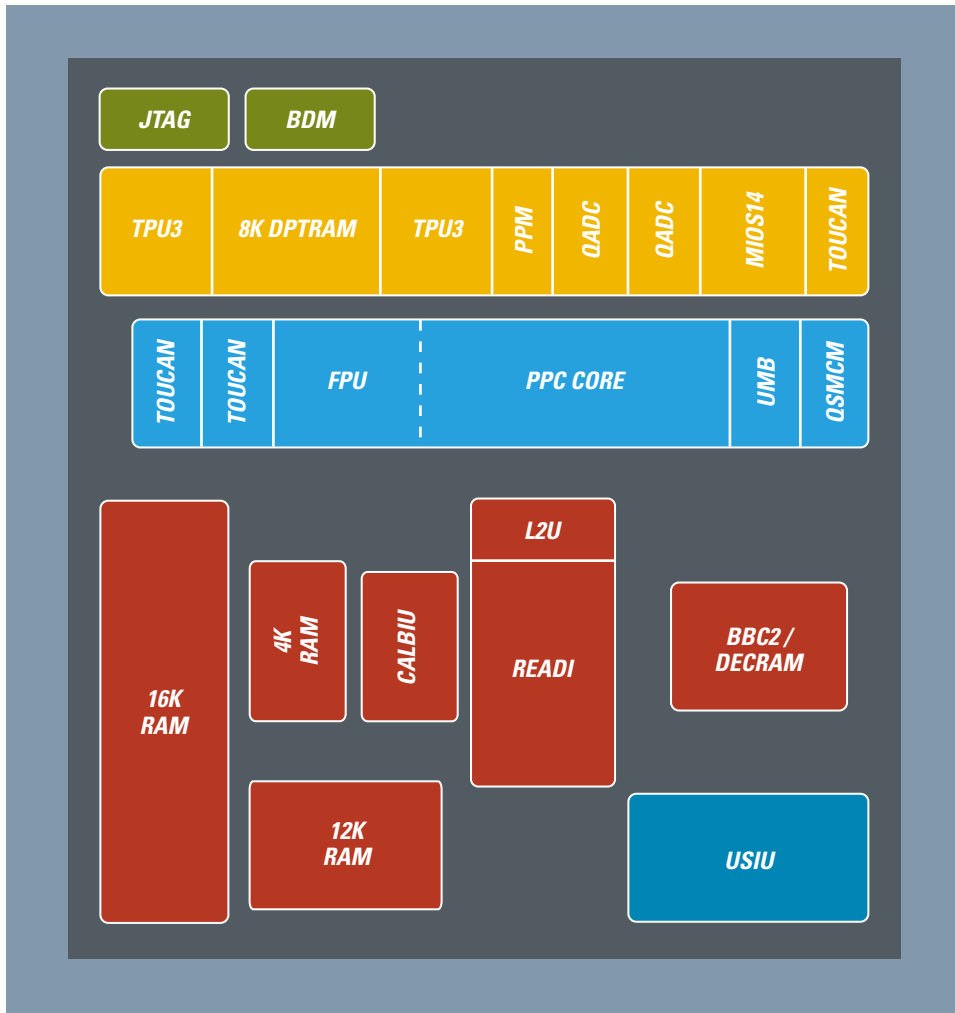
**PROTECT YOUR
TECHNOLOGY INVESTMENTS**

All members of the MPC500 family from Motorola have a clear migration path between products and from previous generations so you can cost effectively adopt or upgrade your products as your needs change.

The MPC561 leverages a full set of development tools and operating systems already available for this computing platform. JTAG and background debug

mode (BDM) come on all of the MPC500 family members, giving you the means to perform production testing without having to be a processor expert. The BDM is designed to allow you to develop and easily debug application software in the development system of the targeted application. Additionally, with the industry-standard interface READI (NEXUS) module, you have the capability to support additional features.

**For More Information On This Product,
Go to: www.freescale.com**



- Queued Serial Multi-Channel Module (QSMCM) with 1 Queued Serial Peripheral Interface (QSPI) and 2 Serial Communication Interfaces (SCI)
- Two enhanced QADC64 modules with legacy mode support (32 channels)

**MOTOROLA MPC561
BENEFITS**

- Cost-effective performance for complex applications not requiring embedded flash or large memory arrays
- Low development costs
- Quick time-to-market
- Code capability and scalability among family members and between generations helps to eliminate migration worries, additionally providing software reuse between family members.

**COMMITTED TO YOU FOR
THE LONG RUN**

With 30 years of leadership in electronics, Motorola understands your priorities – design higher performance products in less time and at a reduced total cost. To that end, the MPC500 family of microcontrollers, including the MPC561, enables you to buy as much or as little performance as you need to help meet your product development goals.

Learn more about the MPC561.
Visit our Web site at:
www.motorola.com/semiconductors

**MOTOROLA MPC561
FEATURES**

- MPC500 core with Floating Point Unit – compliant with the PowerPC instruction set architecture
- 32K bytes of static RAM with 8K bytes of DPTRAM (which can be shared by

TPUs for customized TPU code) and 2K bytes of DEGRAM available for additional RAM used for compression tables on the compression parts (MPC562, MPC564 and MPC566) or otherwise used as SRAM

- 40 or 56 MHz operation
- IRAMSTBY voltage regulator permits retention of SRAM data in low power mode
- Available in both industrial temperature (-40° C to +85° C) and automotive temperature ranges (-40° C to +125° C)
- Four low power modes: On, doze, sleep, deep sleep, and power-down
- NEXUS debug port (class 3) – IEEE-ISTO 5001 - 1999
- Dual Time Processor Units (Type 3)
- Three TouCAN™ (CAN 2.0B) controller modules
- 5V general purpose I/O
- Modular I/O Subsystem (MIOS) module provides 22-timer channels and 16 general purpose I/O