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SEMICONDUCTOR®

October 2013

FQD2N100 / FQU2N100

N-Channel QFET® MOSFET

1000 V, 1.6 A, 9 Ω

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 1.6 A, 1000 V, $R_{DS(on)}$ = 9 Ω (Max.)@ V_{GS} = 10 V, I_D = 0.8 A
- Low Gate Charge (Typ. 12 nC)
- Low Crss (Typ. 5 pF)
- 100% Avalanche Tested
- RoHS Compliant

D-PAK   I-PAK
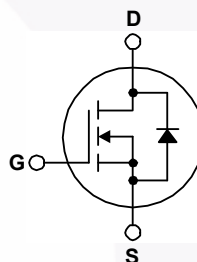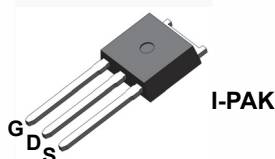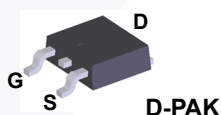
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

| Symbol	Parameter			FQD2N100TM / FQU2N100TU	Unit
V_{DSS}	Drain-Source Voltage			1000	V
I_D	Drain Current	- Continuous (T_C = 25°C)		1.6	A
		- Continuous (T_C = 100°C)		1.0	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	6.4	A
V_{GSS}	Gate-Source Voltage			± 30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	160	mJ
I_{AR}	Avalanche Current		(Note 1)	1.6	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	5.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *			2.5	W
	Power Dissipation (T_C = 25°C)			50	W
	- Derate above 25°C			0.4	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FQD2N100TM FQU2N100TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	110	
	Thermal Resistance, Junction to Ambient (* 1 in^2 pad of 2 oz copper), Max.	50	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD2N100	FQD2N100TM	DPAK	330 mm	16 mm	2500
FQU2N100	FQU2N100TU	IPAK	-	-	70

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	1000	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.976	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 1000 V, V_{GS} = 0 V	--	--	10	µA
		V_{DS} = 800 V, T_C = 125°C	--	--	100	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.8 A	--	7.1	9	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 0.8 A	--	1.9	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	400	520	pF
C_{oss}	Output Capacitance		--	40	52	pF
C_{rss}	Reverse Transfer Capacitance		--	5	6.5	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 500 V, I_D = 2.0 A, R_G = 25 Ω	--	13	35	ns
t_r	Turn-On Rise Time		--	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	60	ns
t_f	Turn-Off Fall Time	(Note 4)	--	35	80	ns
Q_g	Total Gate Charge	V_{DS} = 800 V, I_D = 2.0 A, V_{GS} = 10 V	--	12	15.5	nC
Q_{gs}	Gate-Source Charge		--	2.5	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	6.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	6.0	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.6 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2.0 A, dI_F / dt = 100 A/µs	--	520	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.3	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 120mH, I_{AS} = 1.6A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 2.0A, di/dt ≤ 300A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Essentially independent of operating temperature

Typical Characteristics
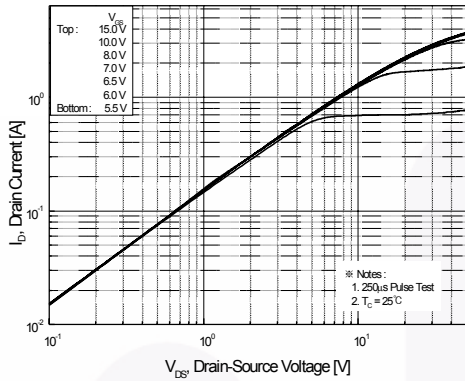
Figure 1. On-Region Characteristics
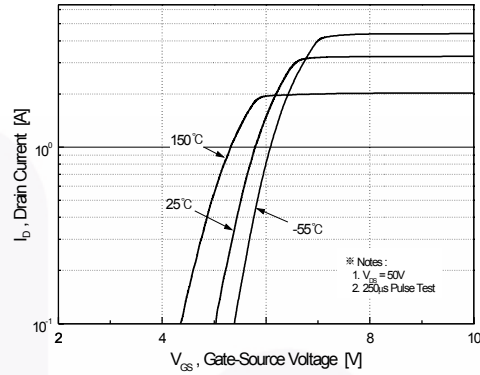
Figure 2. Transfer Characteristics
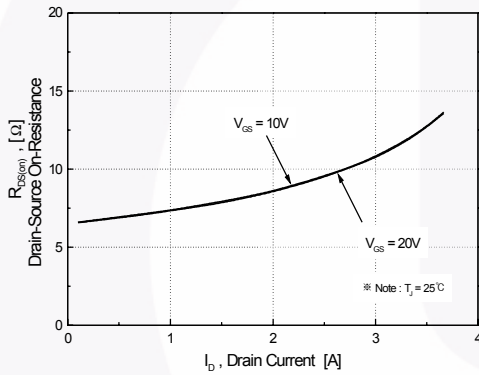
Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage
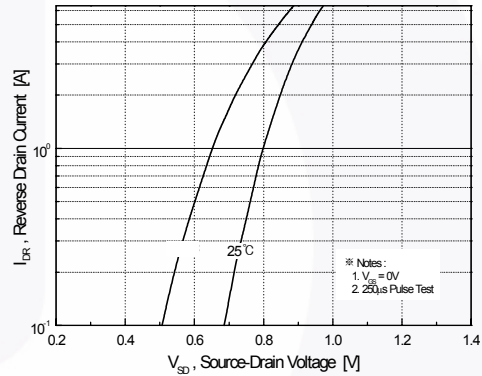
Figure 4. Body Diode Forward Voltage
Variation vs. Source Current and
Temperature
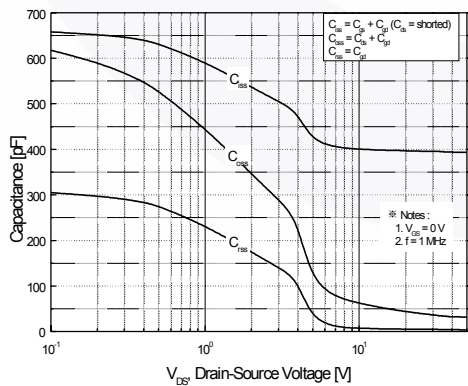
Figure 5. Capacitance Characteristics
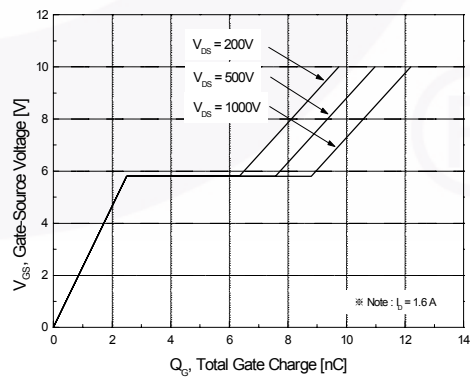
Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)
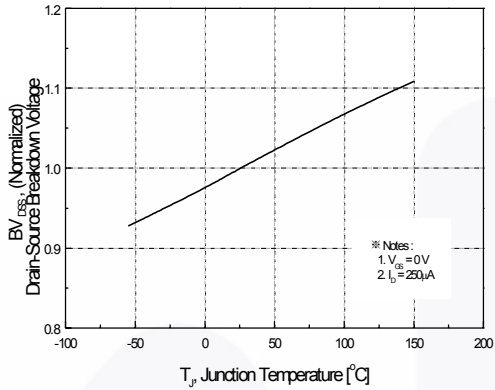
Figure 7. Breakdown Voltage Variation vs. Temperature
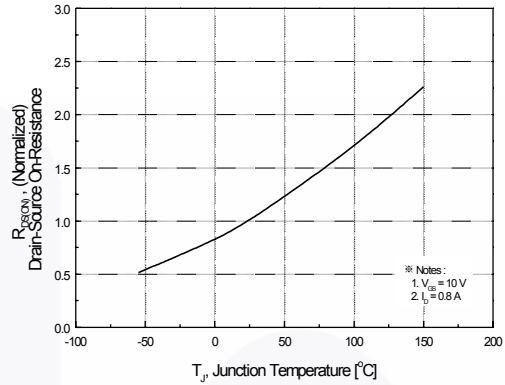
Figure 8. On-Resistance Variation vs. Temperature
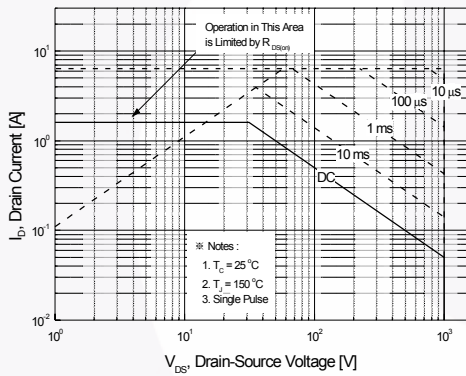
Figure 9. Maximum Safe Operating Area
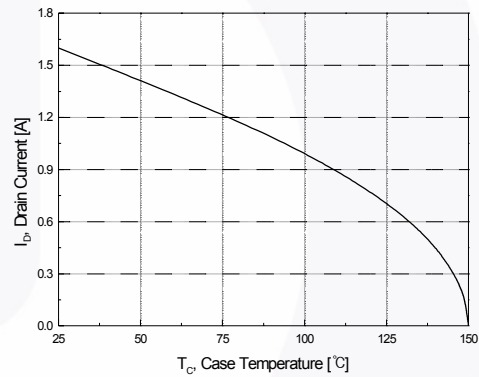
Figure 10. Maximum Drain Current vs. Case Temperature
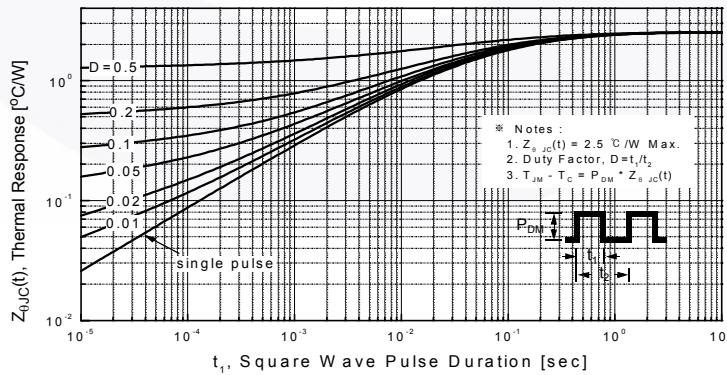
Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform
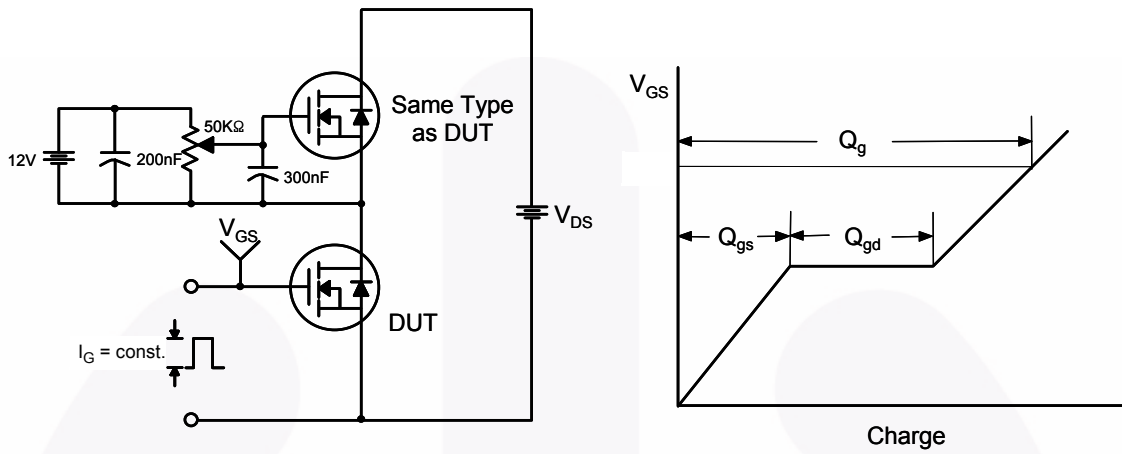
Figure 13. Resistive Switching Test Circuit & Waveforms
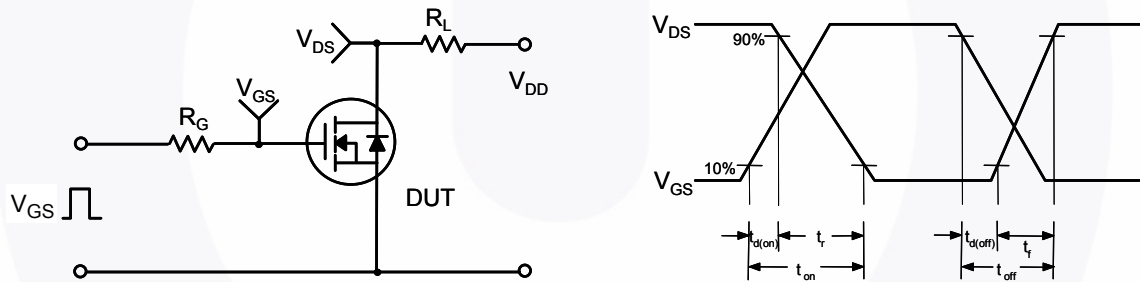
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \; \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop
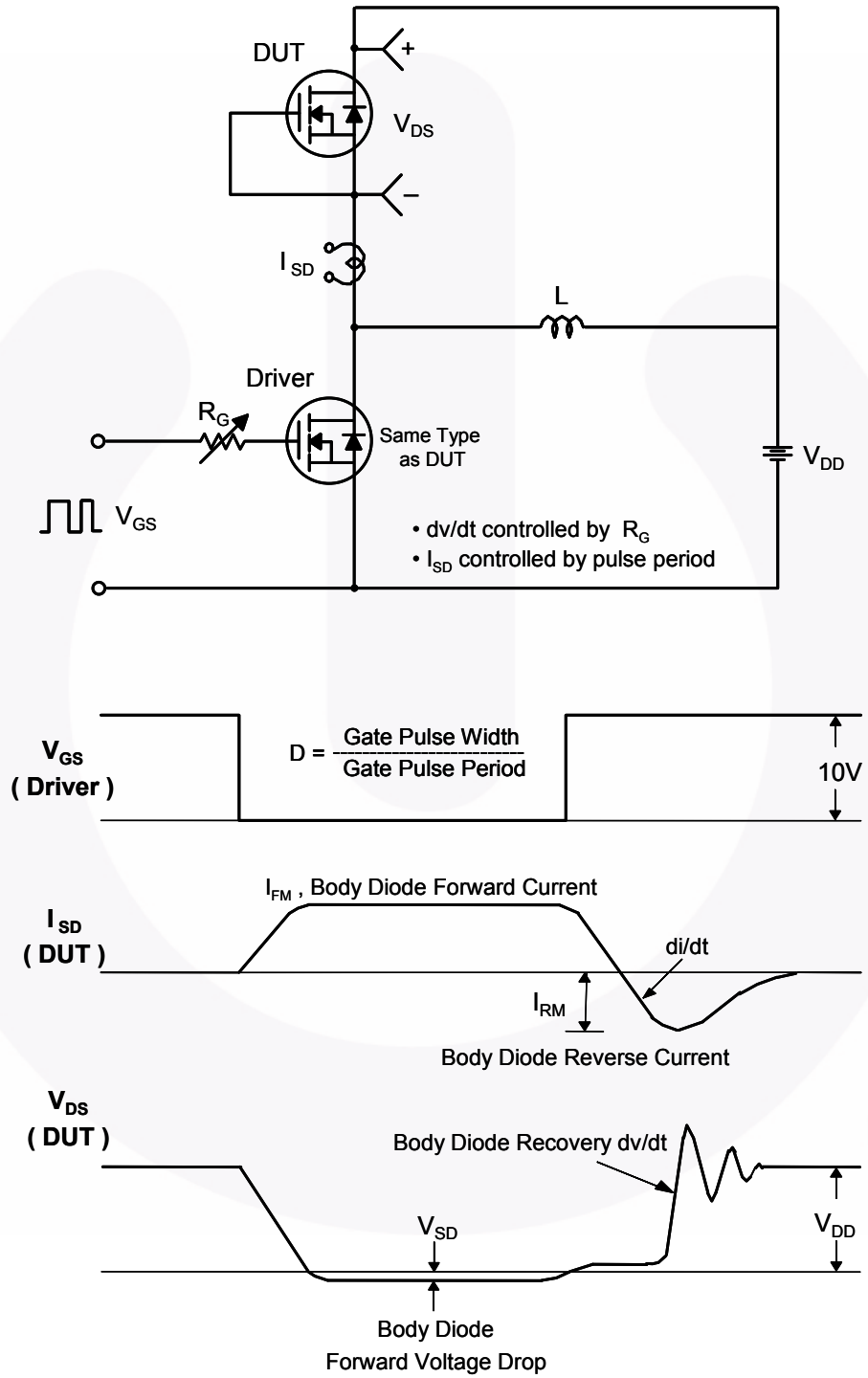
Mechanical Dimensions

TO-252 3L (DPAK)
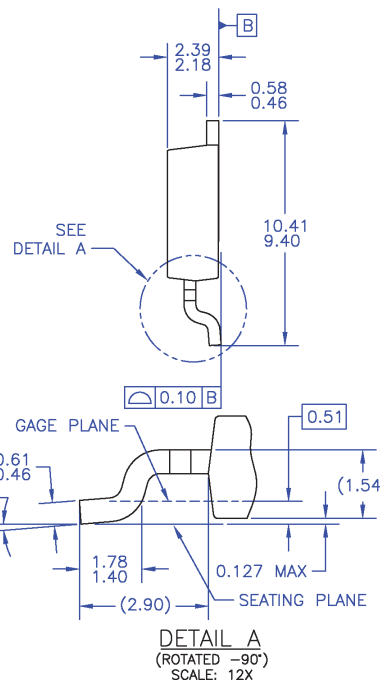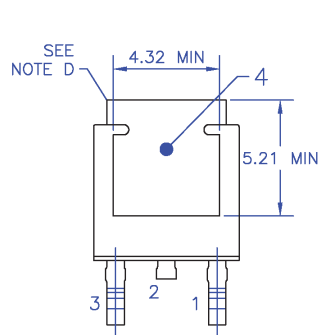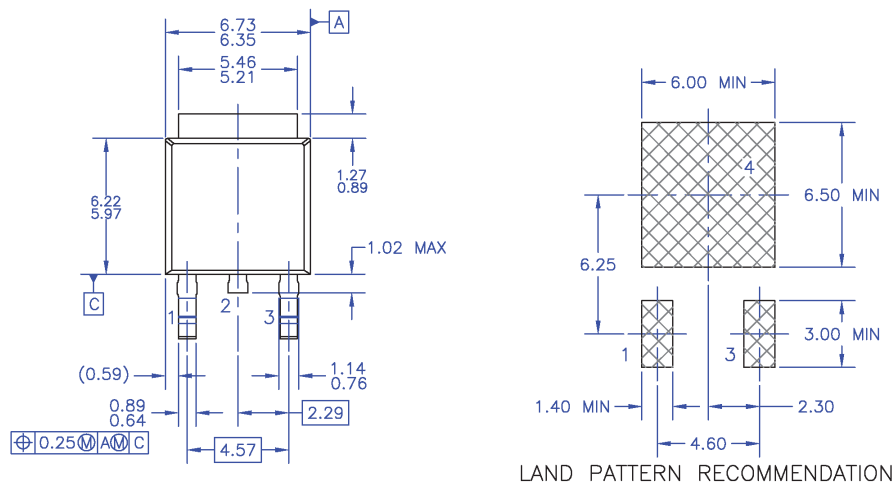
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO−252,
   ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
   ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED
   CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD
   IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSIVE OF BURSS,
   MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD
   TO220P1003X238−3N.
H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

Figure 16. TO252 (D-PAK), Molded, 3 Lead, Option AA&AB

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Dimension in Millimeters

Mechanical Dimensions

TO-251 3L (IPAK)

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) THIS PACKAGE CONFORMS TO JEDEC, TO-251,
   ISSUE C, VARIATION AA, DATED SEP 1988.
C) DIMENSIONING AND TOLERANCING PER
   ASME Y14.5M-1994.
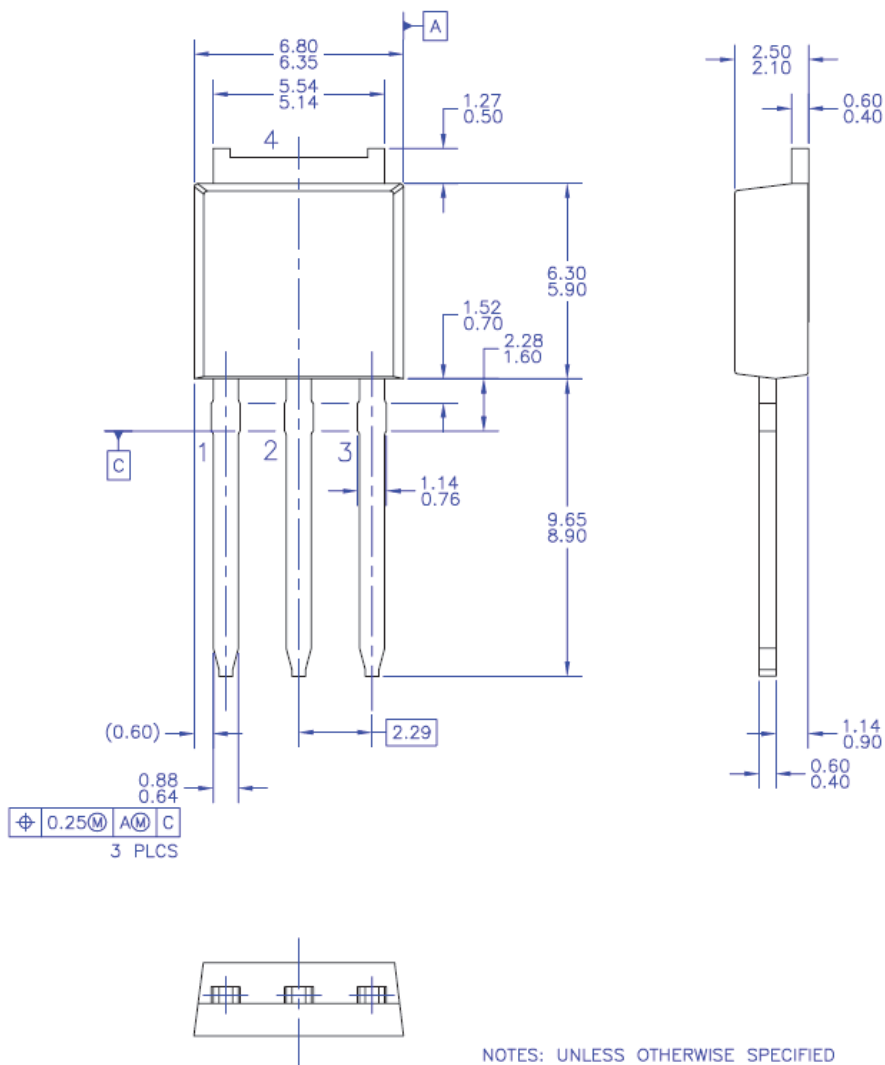
Figure 17. TO-251 (I-PAK) Molded, 3 Lead Option AA

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Dimension in Millimeters

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