340kHz 18V 2A SYNCHRONOUS DC/DC BUCK CONVERTER

Description

The AP6502 is a 340kHz switching frequency external compensated synchronous DC/DC buck converter. It has integrated low R_{DSON} high and low side MOSFETs.

The AP6502 enables continues load current of up to 2A with efficiency as high as 95%.

The AP6502 features current mode control operation, which enables fast transient response times and easy loop stabilization.

The AP6502 simplifies board layout and reduces space requirements with its high level of integration and minimal need for external components, making it ideal for distributed power architectures.

The AP6502 is available in a standard Green SO-8 and SO-8EP package with exposed PAD for improved thermal performance and is RoHS compliant.

Pin Assignments

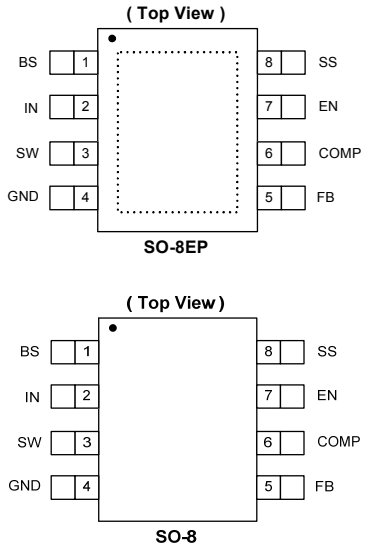


Figure 1 Package Pin Out

Features

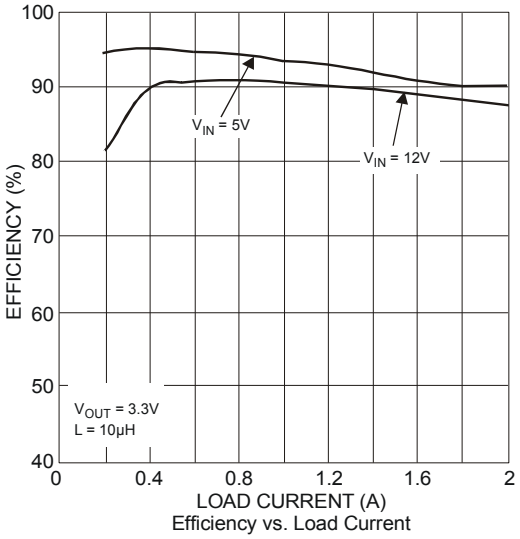
- V_{IN} 4.7V to 18V
- 2A Continuous Output Current, 3A Peak
- V_{OUT} Adjustable from 0.925V to 16V
- 340kHz Switching Frequency
- Programmable Soft-Start
- Enable Pin
- Protection
  - OCP
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Gaming Consoles
- Flat Screen TV Sets and Monitors
- Set Top Boxes
- Distributed power systems
- Home Audio
- Consumer Electronics
- Network Systems
- FPGA, DSP and ASIC Supplies
- Green Electronics

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit



Efficiency vs. Load Current

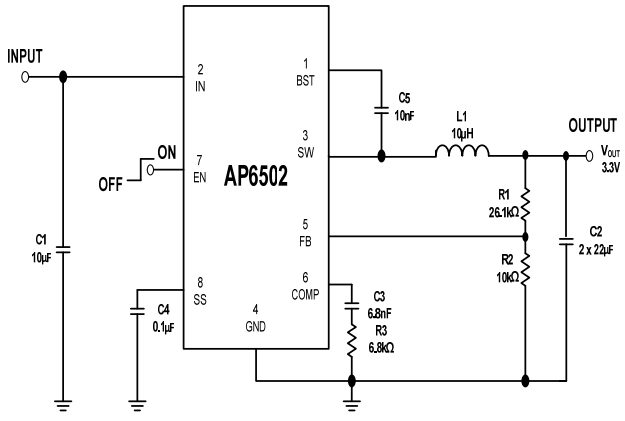


Figure 2 Typical Application Circuit

Pin Descriptions

Pin Number	Pin Name	Function
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01μF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.7V to 18V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground (Connect the exposed pad to Pin 4).
5	FB	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage. The feedback threshold is 0.925V. See Setting the Output Voltage.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required. See Compensation Components.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Attach to IN with a 100kΩ pull up resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS floating.
EP	EP	EP exposed thermal pad connect to Pin 4 GND, not applicable in the SO-8 package.

Functional Block Diagram

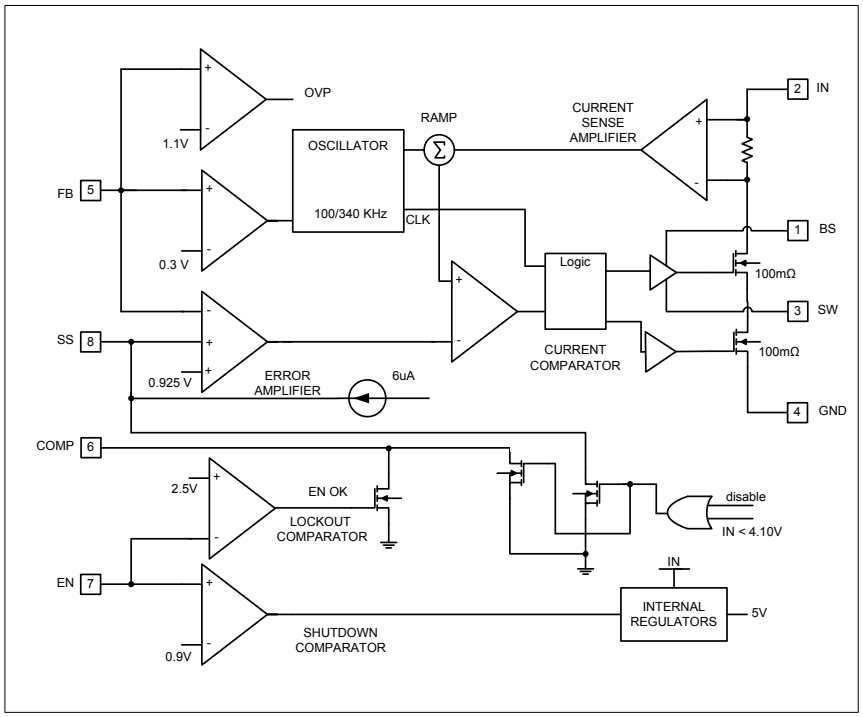


Figure 3 Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to +20	V
V_{SW}	Switch Node Voltage	-1.0 to V_{IN} +0.3	V
V_{BS}	Bootstrap Voltage	V_{SW} -0.3 to V_{SW} +6	V
V_{FB}	Feedback Voltage	-0.3 to +6	V
V_{EN}	Enable/UVLO Voltage	-0.3 to +6	V
V_{COMP}	Comp Voltage	-0.3 to +6	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	3	kV
MM	Machine Model	250	V

Notes: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Rating	Unit
θ_{JA}	Junction to Ambient	SO-8EP	74	°C/W
		SO-8	126	
θ_{JC}	Junction to Case	SO-8EP	16	
		SO-8	28	

Note: 6. Test condition: SO-8: Device mounted on 1"x1" FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
SO-8EP: Device mounted on 1" x 1" FR-4 substrate PC board, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Recommended Operating Conditions (Note 7) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	4.7	18	V
T_A	Operating Ambient Temperature Range	-40	+85	°C

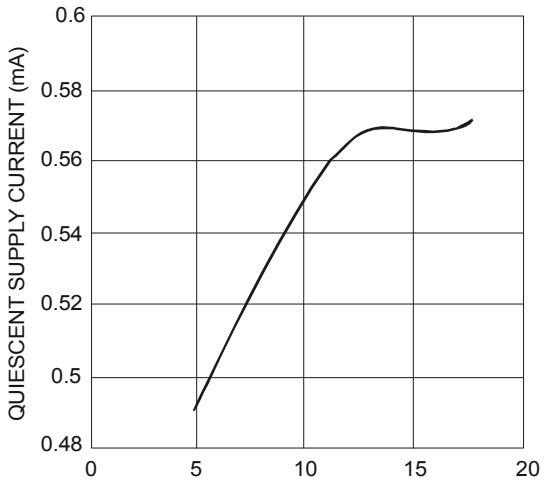
Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (V_{IN} = 12V, @T_A = +25°C, unless otherwise specified.)

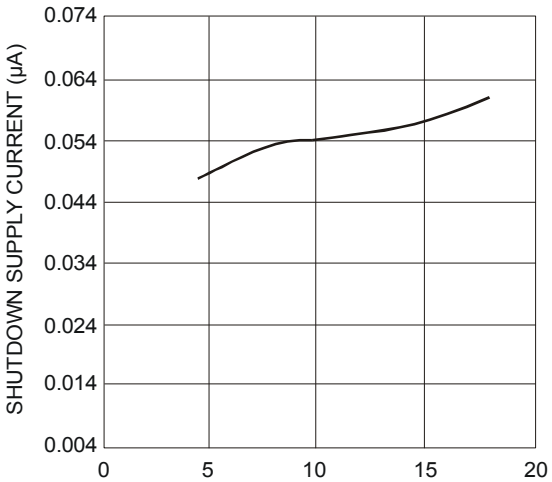
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{IN}	Shutdown Supply Current	V_{EN} = 0V		0.3	3.0	μA
I_{IN}	Supply Current (Quiescent)	V_{EN} = 2.0V, V_{FB} = 1.0V		0.6	1.5	mA
$R_{DS(ON)1}$	High-Side Switch On-Resistance (Note 8)			130		mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance (Note 8)			130		mΩ
I_{LIMIT}	HS Current Limit	Minimum duty cycle		4.4		A
I_{LIMIT}	LS Current Limit	From Drain to Source		0.9		A
	High-Side Switch Leakage Current	V_{EN} = 0V, V_{SW} = 0V, V_{SW} = 12V		0	10	μA
AVEA	Error Amplifier Voltage Gain (Note 8)			800		V/V
GEA	Error Amplifier Transconductance	ΔI_C = ±10μA		1000		μA/V
GCS	COMP to Current Sense Transconductance			2.8		A/V
F_{SW}	Oscillator Frequency	V_{FB} = 0.75V	300	340	380	kHz
F_{FB}	Fold-back Frequency	V_{FB} = 0V		0.30		f_{SW}
D_{MAX}	Maximum Duty Cycle	V_{FB} = 800mV		90		%
T_{ON}	Minimum On Time			130		ns
V_{FB}	Feedback Voltage	T_A = -40°C to +85°C	900	925	950	mV
	Feedback Overvoltage Threshold			1.1		V
V_{EN_Rising}	EN Rising Threshold		0.7	0.8	0.9	V
	EN Lockout Threshold Voltage		2.2	2.5	2.7	V
	EN Lockout Hysteresis			220		mV
$INUV_{Vth}$	V_{IN} Under Voltage Threshold Rising		3.80	4.05	4.40	V
$INUV_{HYS}$	V_{IN} Under Voltage Threshold Hysteresis			250		mV
	Soft-Start Current	V_{SS} = 0V		6		μA
	Soft-Start Period	C_{SS} = 0.1μF		15		ms
T_{SD}	Thermal Shutdown (Note 8)			160		°C

Note: 8. Guaranteed by design

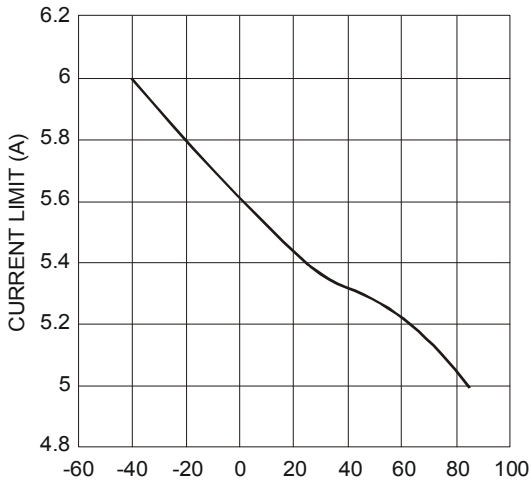
Typical Performance Graphs (V_{IN} = 12V, @T_A = +25°C, unless otherwise specified.)



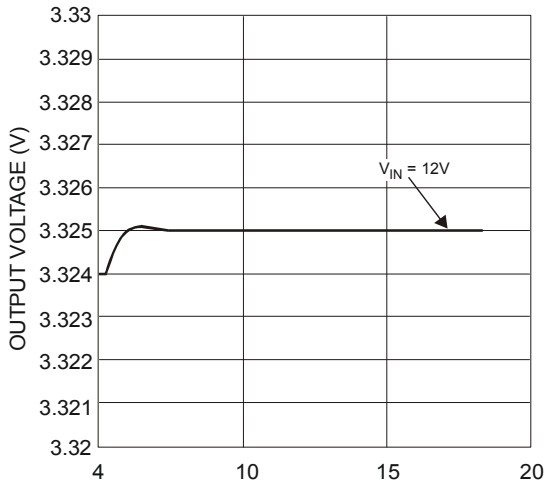
Quiescent Supply Current vs. Input Voltage



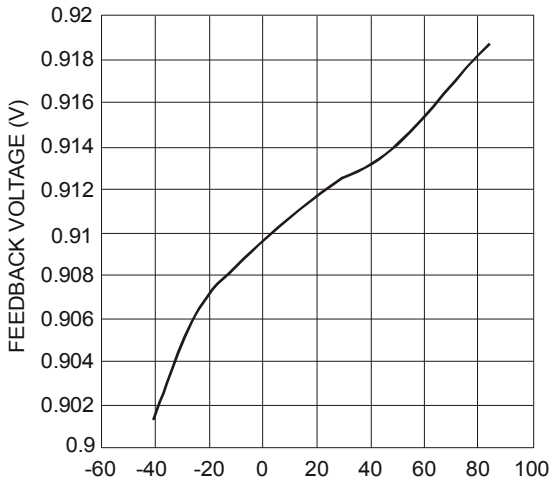
Shutdown Supply Current vs. Input Voltage



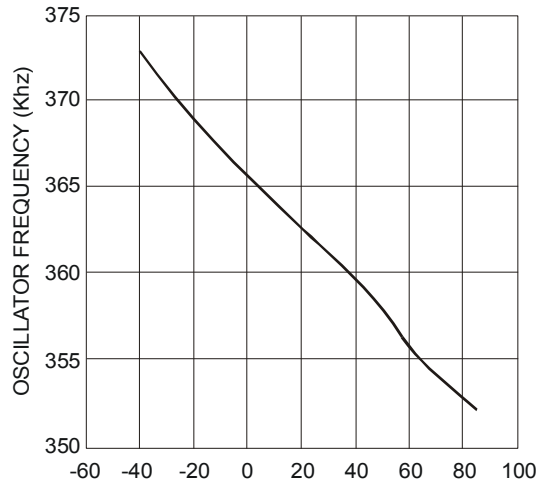
Current Limit vs. Temperature



Line Regulation

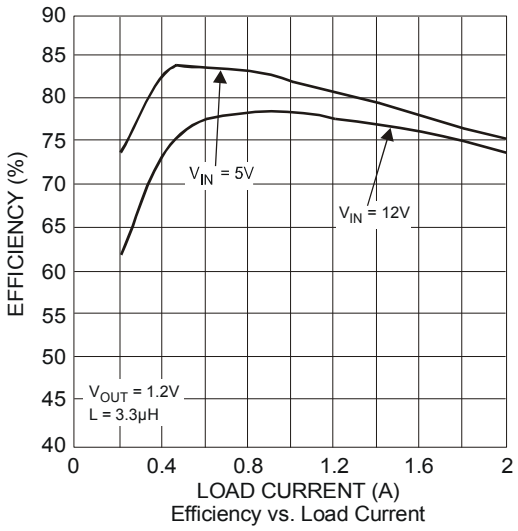


Feedback Voltage vs. Temperature

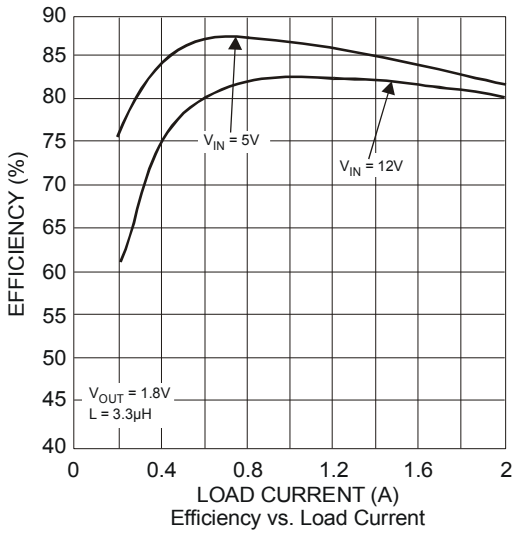


Oscillator Frequency vs. Temperature

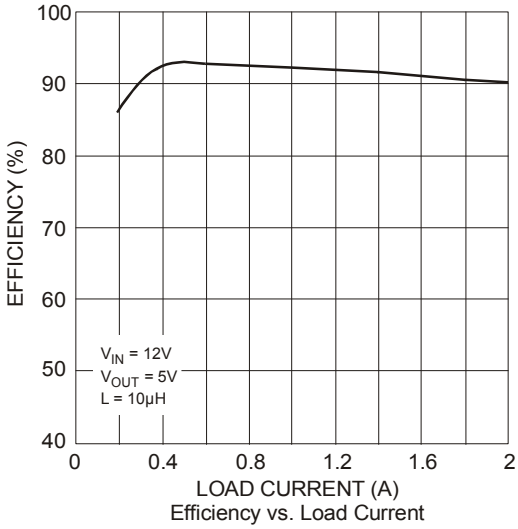
Typical Performance Graphs (cont.) (V_{IN} = 12V, V_{OUT} = 3.3V, (@T_A = +25°C, unless otherwise specified.)



Efficiency vs. Load Current



Efficiency vs. Load Current

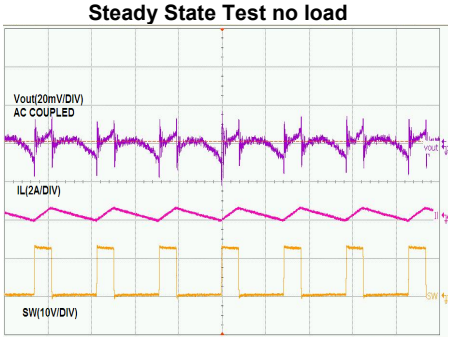


Efficiency vs. Load Current

Typical Performance Characteristics

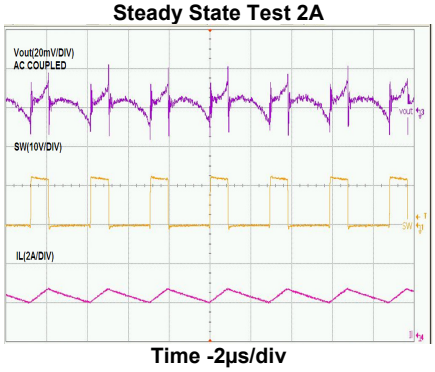
(V_{IN} = 12V, V_{OUT} = 3.3V, L = 10μH, C1 = 22μF, C2 = 47μF, @T_A = +25°C, unless otherwise specified.)

Steady State Test no load



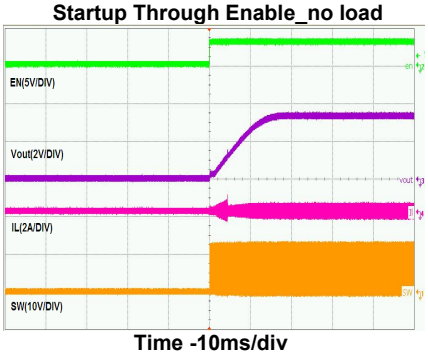
Time -2μs/div

Steady State Test 2A



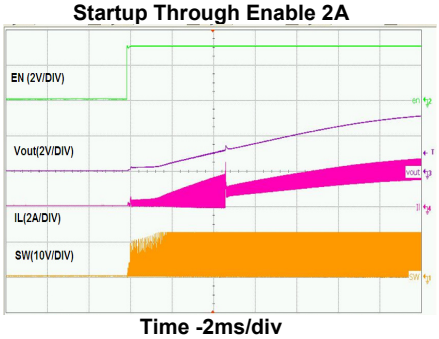
Time -2μs/div

Startup Through Enable_no load



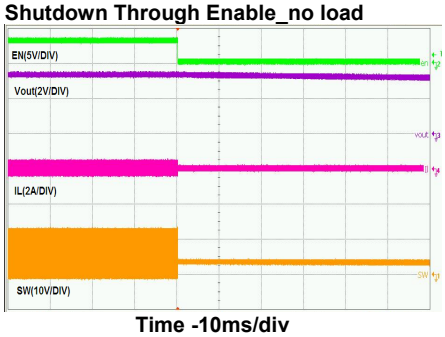
Time -10ms/div

Startup Through Enable 2A



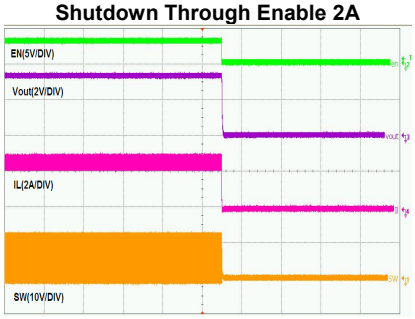
Time -2ms/div

Shutdown Through Enable_no load



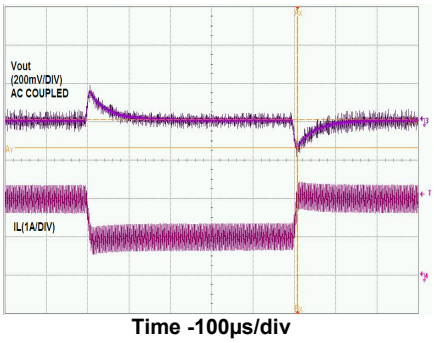
Time -10ms/div

Shutdown Through Enable 2A



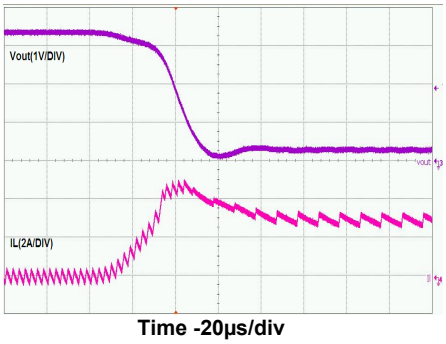
Time -5ms/div

Load Transient Test 1.0A to 2.0A



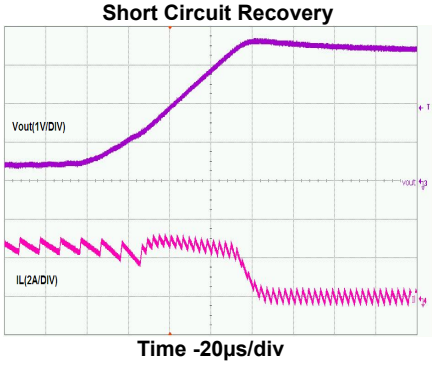
Time -100μs/div

Short Circuit Test



Time -20μs/div

Short Circuit Recovery



Time -20μs/div

Applications Information

Theory of Operation

The AP6502 is a 2A current mode control, synchronous buck regulator with built in power MOSFETs. Current mode control assures excellent line and load regulation and a wide loop bandwidth for fast response to load transients. Figure 3 depicts the functional block diagram of AP6502.

The operation of one switching cycle can be explained as follows. At the beginning of each cycle, HS (high-side) MOSFET is off. The error amplifier (EA) output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 340kHz oscillator clock signal sets the RS Flip-Flop. Its output turns on HS MOSFET. The current sense amplifier is reset for every switching cycle.

When the HS MOSFET is on, inductor current starts to increase. The current sense amplifier senses and amplifies the inductor current. Since the current mode control is subject to sub-harmonic oscillations that peak at half the switching frequency, ramp slope compensation is utilized. This will help to stabilize the power supply. This ramp compensation is summed to the current sense amplifier output and compared to the error amplifier output by the PWM comparator. When the sum of the current sense amplifier output and the slope compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and HS MOSFET is turned off.

For one whole cycle, if the sum of the current sense amplifier output and the slope compensation signal does not exceed the EA output, then the falling edge of the oscillator clock resets the Flip-Flop. The output of the error amplifier increases when feedback voltage (VFB) is lower than the reference voltage of 0.925V. This also increases the inductor current as it is proportional to the EA voltage.
If in one cycle the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off. When the HS MOSFET turns off, the synchronous LS MOSFET turns on until the next clock cycle begins. There is a "dead time" between the HS turn off and LS turn on that prevents the switches from "shooting through" from the input supply to ground.

The voltage loop is compensated through an internal transconductance amplifier and can be adjusted through the external compensation components.

Enable

Above the 'EN Rising Threshold', the internal regulator is turned on and the quiescent current can be measured above this threshold. The enable (EN) input allows the user to control turning on or off the regulator. To enable the AP6502, EN must be pulled above the 'EN Lockout Threshold Voltage' and to disable the AP6502, EN must be pulled below 'EN Lockout Threshold Voltage - EN Lockout Hysteresis' (2.2V-0.22V =1.98V).

External Soft Start

Soft start is traditionally implemented to prevent the excess inrush current. This in turn prevents the converter output voltage from overshooting when it reaches regulation. The AP6502 has an internal current source with a soft start capacitor to ramp the reference voltage from 0V to 0.925V. The soft start current is 6uA. The soft start sequence is reset when there is a Thermal Shutdown, Under Voltage Lockout (UVLO) or when the part is disabled using the EN pin.
External Soft Start can be calculated from the formula below:

$$I_{SS} = C * \frac{DV}{DT}$$

Where;

I_{SS} = Soft Start Current
C = External Capacitor
DV = change in feedback voltage from 0V to maximum voltage
DT = Soft Start Time

Current Limit Protection

In order to reduce the total power dissipation and to protect the application, AP6502 has cycle-by-cycle current limiting implementation. The voltage drop across the internal high-side MOSFET is sensed and compared with the internally set current limit threshold. This voltage drop is sensed at about 30ns after the HS turns on. When the peak inductor current exceeds the set current limit threshold, current limit protection is activated. During this time the feedback voltage (VFB) drops down. When the voltage at the FB pin reaches 0.3V, the internal oscillator shifts the frequency from the normal operating frequency of 340kHz to a fold-back frequency of 102kHz. The current limit is reduced to 70% of nominal current limit when the part is operating at 102kHz. This low fold-back frequency prevents runaway current.

Applications Information (cont.)

Under Voltage Lockout (UVLO)

Under Voltage Lockout is implemented to prevent the IC from insufficient input voltages. The AP6502 has a UVLO comparator that monitors the input voltage and the internal bandgap reference. If the input voltage falls below 4.0V, the AP6502 will latch an under voltage fault. In this event the output will be pulled low and power has to be re-cycled to reset the UVLO fault.

Over Voltage Protection

When the AP6502 FB pin exceeds 20% of the nominal regulation voltage of 0.925V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

Thermal Shutdown

The AP6502 has on-chip thermal protection that prevents damage to the IC when the die temperature exceeds safe margins. It implements a thermal sensing to monitor the operating junction temperature of the IC. Once the die temperature rises to approximately +160°C, the thermal protection feature gets activated. The internal thermal sense circuitry turns the IC off thus preventing the power switch from damage.
A hysteresis in the thermal sense circuit allows the device to cool down to approximately +120°C before the IC is enabled again through soft start. This thermal hysteresis feature prevents undesirable oscillations of the thermal protection circuit.

Setting the Output Voltage

The output voltage can be adjusted from 0.925V to 16V using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages. Resistor R1 is selected based on a design tradeoff between efficiency and output voltage accuracy. For high values of R1 there is less current consumption in the feedback network. However the trade off is output voltage accuracy due to the bias current in the error amplifier. R1 can be determined by the following equation:

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{0.925} - 1 \right)$$

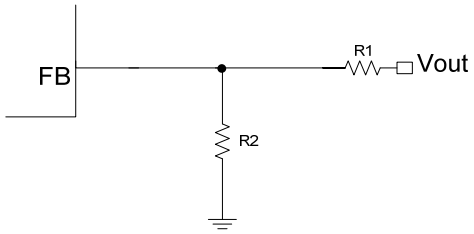


Figure 4 Feedback Divider Network

When output voltage is low, network as shown in Figure 4 is recommended.

Table 1 – Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
5	45.3	10
3.3	26.1	10
2.5	16.9	10
1.8	9.53	10
1.2	3	10

Compensation Components

The AP6502 has an external COMP pin through which system stability and transient response can be controlled. COMP pin is the output of the internal trans-conductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage (0.925V), R_{LOAD} is the load resistor value, G_{CS} is the current sense trans-conductance and A_{VEA} is the error amplifier voltage gain.

Applications Information (cont.)

Compensation Components (cont.)

The control loop transfer function incorporates two poles one is due to the compensation capacitor (C3) and the output resistor of error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier trans-conductance.

One zero is present due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is crucial.

A rule of thumb is to set the crossover frequency to below one-tenth of the switching frequency. Use the following procedure to optimize the compensation components:

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times fc}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \times C2 \times 0.1 \times fs}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the crossover frequency, which is typically less than one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin set the compensation zero, f_{Z1}, to below one fourth of the crossover frequency to provide sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{2}{\pi \times R3 \times fc}$$

Where R3 is the compensation resistor value.

V_{OUT} (V)	C_{IN}/C1 (µF)	C_{OUT}/C2 (µF)	R_C/R3 (kΩ)	C_C/C3 (nF)	L1 (µH)
1.2	22	47	3.24	6.8	3.3
1.8	22	47	6.8	6.8	3.3
2.5	22	47	6.8	6.8	10
3.3	22	47	6.8	6.8	10
5	22	47	6.8	6.8	10
12	22	47	6.8	6.8	15

Table 2 – Recommended Component Selection

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value;

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}}$$

Where ΔI_L is the inductor ripple current.

And f_{SW} is the buck converter switching frequency.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Applications Information (cont.)

Inductor (cont.)

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence choosing an inductor with appropriate saturation current rating is important.

A 1µH to 10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications.

For highest efficiency, the inductor's DC resistance should be less than 200mΩ. Use a larger inductance for improved efficiency under light load conditions.

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on time on the upper MOSFET. It must hence have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has RMs rating that is greater than half of the maximum load current.

Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur. For most applications, a 4.7µF ceramic capacitor is sufficient.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

Maximum capacitance required can be calculated from the following equation:
ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated from the equation below:

$$Vout_{capacitor} = \Delta I_{inductor} * ESR$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, a 22µF ceramic capacitor will be sufficient.

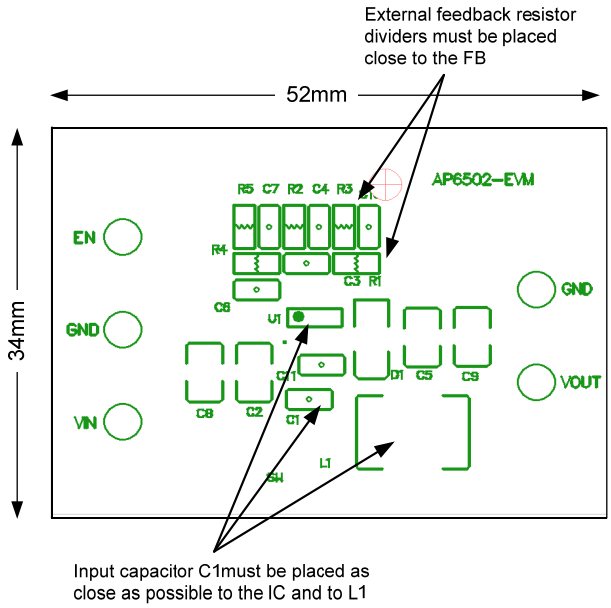
$$C_o = \frac{L(I_{out} + \frac{\Delta I_{inductor}}{2})^2}{(\Delta V + V_{out})^2 - V_{out}^2}$$

Where ΔV is the maximum output voltage overshoot.

Applications Information (cont.)

PC Board Layout

This is a high switching frequency converter. Hence attention must be paid to the switching currents interference in the layout. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces.



AP6502SP-13 is exposed at the bottom of the package and must be soldered directly to a well designed thermal pad on the PCB. This will help to increase the power dissipation. This is not applicable for the AP6502S-13.

External Bootstrap Diode

It is recommended that an external bootstrap diode be added when the input voltage is no greater than 5V or the 5V rail is available in the system. This helps to improve the efficiency of the regulator. This solution is also applicable for D > 65%. The bootstrap diode can be a low cost one such as BAT54 or a schottky that has a low Vf.

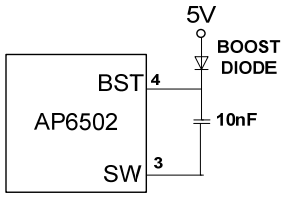
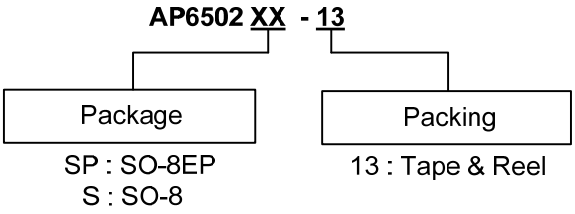


Figure 7—External Bootstrap Compensation Components

Recommended Diodes:

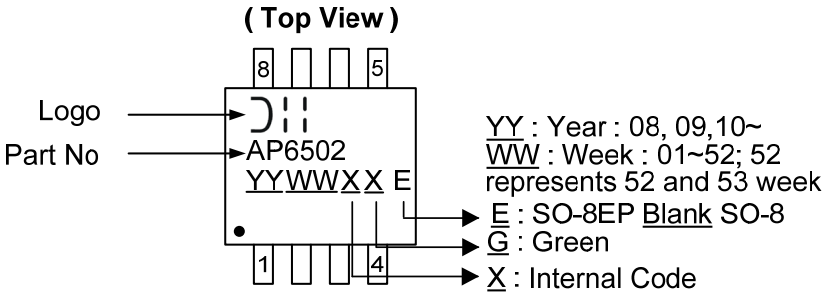
Part Number	Voltage/Current Rating	Vendor
B130	30V, 1A	Diodes Inc
SK13	30V, 1A	Diodes Inc

Ordering Information



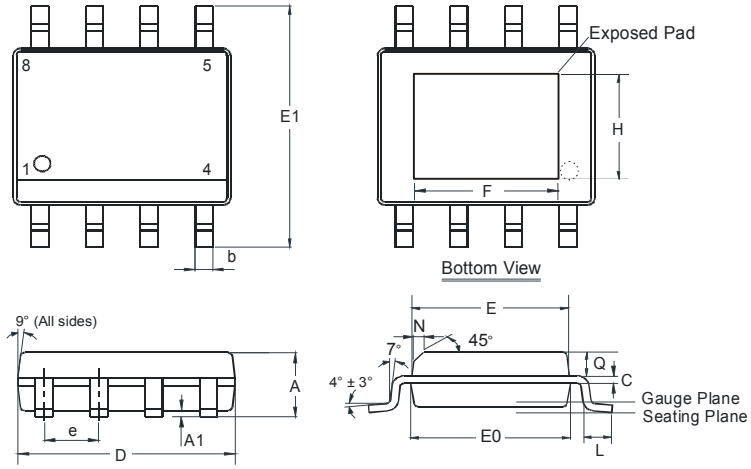
Device	Package Code	Packaging	13" Tape and Reel	
			Quantity	Part Number Suffix
AP6502SP-13	SP	SO-8EP	2500/Tape & Reel	-13
AP6502S-13	S	SO-8	2500/Tape & Reel	-13

Marking Information



Package Outline Dimensions (All dimensions in mm.)

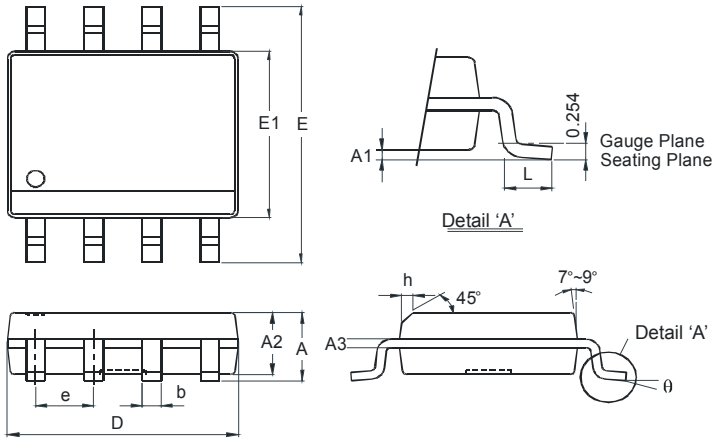
(1) SO-8EP



SO-8EP (SOP-8L-EP)			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Package Outline Dimensions (cont.) (All dimensions in mm.)

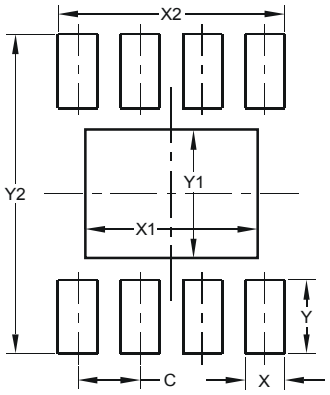
(2) SO-8



SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

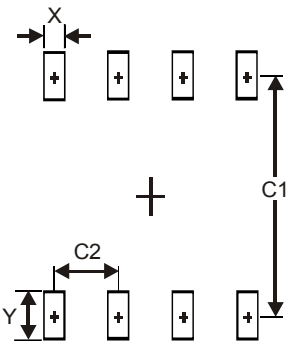
Suggested Pad Layout (All dimensions in mm.)

(1) SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

(2) SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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