CY22392 Automotive

Three-PLL General Purpose Flash Programmable Clock Generator

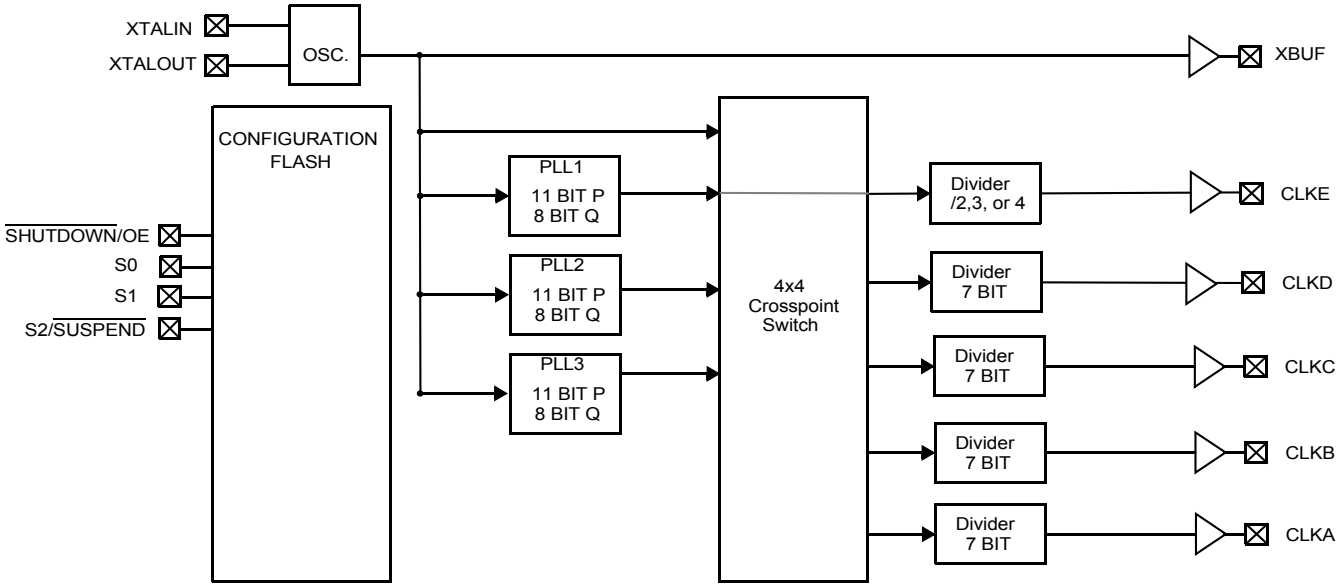
Features

- Three Integrated Phase-locked Loops
- Ultra Wide Divide Counters (8-bit Q, 11-bit P, and 7-bit Post Divide)
- Improved Linear Crystal Load Capacitors
- Flash Programmability
- Field Programmable
- Low-jitter, High-accuracy Outputs
- Power Management Options (Shutdown, OE, Suspend)
- Configurable Crystal Drive Strength
- Frequency Select through three External LVTTL Inputs
- 3.3 V Operation
- Automotive A temperature range
- AEC-Q100 Qualified
- 16-pin TSSOP Package
- CyClocksRT™ Support

Benefits

- Generates up to three unique frequencies on six outputs up to 166 MHz from an external source. Functional upgrade for current CY2292 family.
- Enables 0 ppm frequency generation and frequency conversion under the most demanding applications.
- Improves frequency accuracy over temperature, age, process, and initial offset.
- Nonvolatile programming enables easy customization, fast turnaround, performance tweaking, design timing margin testing, inventory control, lower part count, and more secure product supply. In addition, any part in the family can also be programmed multiple times, which reduces programming errors and provides an easy upgrade path for existing designs.
- In-house programming of samples and prototype quantities is available using the CY3672 development kit.
- Performance suitable for high-end multimedia, communications, industrial, A/D Converters, and consumer applications.
- Supports numerous low power application schemes and reduces EMI by enabling unused outputs to be turned off.
- Adjusts crystal drive strength for compatibility with virtually all crystals.
- 3-bit external frequency select options for PLL1, CLKA, and CLKB.
- Industry-standard supply voltage.
- Industry-standard packaging saves on board space.
- Easy to use software support for design entry.

Logic Block Diagram

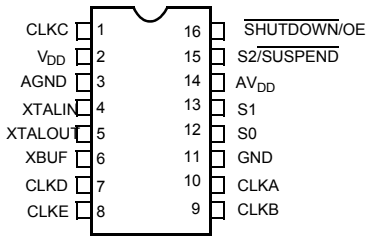


Contents

Pin Configurations **3**
Pin Definitions **3**
Operation **4**
Configurable PLLs 4
General Purpose Inputs 4
Crystal Input 4
Output Configuration 4
Power Saving Features 4
Improving Jitter 5
Power Supply Sequencing 5
CyberClocks™ Software **5**
Device Programming **5**
Junction Temperature Limitations **5**
Maximum Ratings **6**
Operating Conditions **6**
Electrical Characteristics **6**
Switching Characteristics **7**
Switching Waveforms **8**
Test Circuit **8**
Ordering Information **9**
Possible Configurations 9
Ordering Code Definitions 9
Package Diagrams **10**
Acronyms **11**
Document Conventions **11**
Units of Measure 11
Document History Page **12**
Sales, Solutions, and Legal Information **13**
Worldwide Sales and Design Support 13
Products 13
PSoC® Solutions 13
Cypress Developer Community 13
Technical Support 13

Pin Configurations

Figure 1. 16-pin TSSOP pinout



Pin Definitions

Name	Pin Number	Description
CLKC	1	Configurable clock output C
V_{DD}	2	Power supply
AGND	3	Analog Ground
XTALIN	4	Reference crystal input or external reference clock input
XTALOUT	5	Reference crystal feedback
XBUF	6	Buffered reference clock output
CLKD	7	Configurable clock output D
CLKE	8	Configurable clock output E
CLKB	9	Configurable clock output B
CLKA	10	Configurable clock output A
GND	11	Ground
S0	12	General Purpose Input for Frequency Control; bit 0
S1	13	General Purpose Input for Frequency Control; bit 1
AV_{DD}	14	Analog Power Supply
S2/$\overline{\text{SUSPEND}}$	15	General Purpose Input for Frequency Control; bit 2. Optionally Suspend mode control input.
$\overline{\text{SHUTDOWN}}$/OE	16	Places outputs in three-state condition and shuts down chip when Low. Optionally, only places outputs in tristate condition and does not shut down chip when Low.

Operation

The CY22392 is an upgrade to the existing CY2292. The new device has a wider frequency range, greater flexibility, improved performance, and incorporates many features that reduce PLL sensitivity to external system issues.

The device has three PLLs which, when combined with the reference, enable up to four independent frequencies to be output on up to six pins. These three PLLs are completely programmable.

Configurable PLLs

PLL1 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL1 is sent to the crosspoint switch. The output of PLL1 is also sent to a /2, /3, or /4 synchronous post-divider that is output through CLKE. The frequency of PLL1 can be changed by external CMOS inputs, S0, S1, S2. See the following section on General Purpose Inputs for more details.

PLL2 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the crosspoint switch.

PLL3 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL3 is sent to the cross-point switch.

General Purpose Inputs

S0, S1, and S2 are general purpose inputs that can be programmed to enable eight different frequency settings. Options that may be switched with these general purpose inputs are as follows: the frequency of PLL1, the output divider of CLKB, and the output divider of CLKA.

CLKA and CLKB both have 7-bit dividers that point to one of two programmable settings (register 0 and register 1). Both clocks share a single register control, so both must be set to register 0, or both must be set to register 1.

For example, the part may be programmed to use S0, S1, and S2 (0, 0, 0 to 1, 1, 1) to control eight different values of P and Q on PLL1. For each PLL1 P and Q setting, one of the two CLKA and CLKB divider registers can be chosen. Any divider change as a result of switching S0, S1, or S2 is guaranteed to be glitch free.

Crystal Input

The input crystal oscillator is an important feature of this device because of its flexibility and performance features.

The oscillator inverter has programmable drive strength. This enables maximum compatibility with crystals from various manufacturers, processes, performances, and qualities.

The input load capacitors are placed on-die to reduce external component cost. These capacitors are true parallel-plate capacitors for ultra-linear performance. These were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. Non-linear (FET gate) crystal load capacitors must not be used for MPEG, POTS dial tone, communications, or other applications that are sensitive to absolute frequency requirements.

The value of the load capacitors is determined by six bits in a programmable register. The load capacitance can be set with a resolution of 0.375 pF for a total crystal load range of 6 pF to 30 pF.

For driven clock inputs the input load capacitors may be completely bypassed. This enables the clock chip to accept driven frequency inputs up to 166 MHz. If the application requires a driven input, then XTALOUT must be left floating.

Output Configuration

Under normal operation there are four internal frequency sources that may be routed through a programmable crosspoint switch to any of the four programmable 7-bit output dividers. The four sources are: reference, PLL1, PLL2, and PLL3. In addition, many outputs have a unique capability for even greater flexibility. The following is a description of each output.

CLKA's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. Each of the eight possible combinations of S0, S1, S2 controls which of the two programmable registers is loaded into CLKA's 7-bit post divider. See the section General Purpose Inputs for more information.

CLKB's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. Each of the eight possible combinations of S0, S1, and S2 controls which of the two programmable registers is loaded into CLKA's 7-bit post divider. See the section General Purpose Inputs for more information.

CLKC's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.

CLKD's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.

CLKE's output originates from PLL1 and goes through a post divider that may be programmed to /2, /3, or /4.

XBUF is simply the buffered reference.

The clock outputs have been designed to drive a single point load with a total lumped load capacitance of 15 pF. While driving multiple loads is possible with proper termination, it is generally not recommended.

Power Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input tristates the outputs when pulled low. If system shutdown is enabled, a Low on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins is less than 5 μA (typical). After leaving shutdown mode, the PLLs must relock.

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all

associated logic, while suspending an output simply forces a tristate condition.

Improving Jitter

Jitter Optimization Control is useful in mitigating problems related to similar clocks switching at the same moment, causing excess jitter. If one PLL is driving more than one output, the negative phase of the PLL can be selected for one of the outputs (CLKA–CLKD). This prevents the output edges from aligning, enabling superior jitter performance.

Power Supply Sequencing

For parts with multiple V_{DD} pins, there are no power supply sequencing requirements. The part is not fully operational until all V_{DD} pins have been brought up to the voltages specified in the Operating Conditions. All grounds must be connected to the same ground plane.

CyberClocks™ Software

The CyberClocks application enables users to configure this device. Within CyberClocks, select the CyClocksRT tool. The easy-to-use interface offers complete control of the many features of this family including input frequency, PLL, output frequencies, and different functional options. Data sheet frequency range limitations are checked and performance tuning is automatically applied. CyClocksRT also has a power estimation feature that enables you to see the power consumption of your specific configuration. Download a copy of CyberClocks free on Cypress's web site at www.cypress.com. Install and run it on any PC running Windows.

Device Programming

Part numbers starting with CY22392F are 'field programmable' devices. Field programmable devices are shipped unprogrammed, and must be programmed prior to installation on a PCB. After a programming file (.jed) is created using CyberClocks software, devices can be programmed in small quantities using the CY3672 programmer and CY3698 [1] adapter. Programming of the clock device should be done at temperatures < 75 °C. Volume programming is available through Cypress Semiconductor's value added distribution partners or by using third party programmers from BP Microsystems, HiLo Systems, and others. For sufficiently large volumes, Cypress can supply pre-programmed devices with a part number extension that is configuration-specific.

Junction Temperature Limitations

It is possible to program the CY22392 such that the maximum junction temperature rating is exceeded. The package θ_{JA} is 115 °C/W. Use the CyClocksRT power estimation feature to verify that the programmed configuration meets the junction temperature and package power dissipation maximum ratings.

Note
1. Programming of only 16-pin TSSOP package is supported by CY3698.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply Voltage .....–0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to + (AV_{DD} + 0.5 V)

Storage Temperature ..... –65 °C to +125 °C

Junction Temperature
A Grade ..... 125 °C

Data Retention at Tj = 125 °C .....> 10 years

Data Retention at Tj = 150 °C .....> 2 years

Maximum Programming Cycles 100

Package Power Dissipation (A-Grade) ..... 350 mW

Static Discharge Voltage
(per MIL-STD-883, Method 3015) ..... 2000 V

Latch up (according to JEDEC 17) ..... ≥ ±200 mA

Stresses exceeding absolute maximum conditions may cause permanent damage to the device. These conditions are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this data sheet is not implied. Extended exposure to Absolute Maximum Conditions may affect reliability.

Operating Conditions

The following table lists the recommended operating conditions. [2]

Parameter	Description	Min	Typ	Max	Unit
V_{DD}/AV_{DD}	Supply Voltage	3.135	3.3	3.465	V
T_A	Automotive A-Grade Operating Temperature, Ambient	–40	–	+85	°C
f_{REF}	External Reference Crystal	8	–	30	MHz
	External Reference Clock [3], Automotive A-Grade	1	–	166	MHz
t_{PU}	Power up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{OH}	Output High Current [4]	$V_{OH} = V_{DD} – 0.5$ V, V_{DD} = 3.3 V [5]	12	24	–	mA
I_{OL}	Output Low Current [4]	V_{OL} = 0.5 V, V_{DD} = 3.3 V [5]	12	24	–	mA
C_{XTAL_MIN}	Crystal Load Capacitance [4]	Capload at minimum setting	–	6	–	pF
C_{XTAL_MAX}	Crystal Load Capacitance [4]	Capload at maximum setting	–	30	–	pF
C_{LOAD_IN}	Input Pin Capacitance [4]	Except crystal pins	–	7	–	pF
V_{IH}	High Level Input Voltage	CMOS levels,% of AV_{DD}	70%	–	–	AV_{DD}
V_{IL}	Low Level Input Voltage	CMOS levels,% of AV_{DD}	–	–	30%	AV_{DD}
I_{IH}	Input High Current	$V_{IN} = AV_{DD} – 0.3$ V	–	<1	10	µA
I_{IL}	Input Low Current	V_{IN} = +0.3 V	–	<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs (OE = Low)	–	–	10	µA
I_{DD}	Total Power Supply Current under 15 pF load	3.3 V Power Supply; 2 outputs at 166 MHz; 4 outputs at 83 MHz [6]	–	100	–	mA
		3.3 V Power Supply; 2 outputs at 20 MHz; 4 outputs at 40 MHz [6]	–	50	–	mA
I_{DDS}	Total Power Supply Current in Shutdown Mode	Shutdown active	–	5	20	µA

Notes
2. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
3. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
4. Guaranteed by design, not 100% tested.
5. Profile configuration through CyberClocks (JEDEC file) should be so generated such that Drive strength should be at ‘Mid Low’ or above.
6. Profile configuration through CyberClocks (JEDEC file) should be so generated such that for A - Grade, $I_{DDmax} \leq 90$mA (considering T_{Amax} = 85 °C).

Switching Characteristics

Parameter	Name	Description	Min	Typ	Max	Unit
$1/t_1$	Output Frequency under 15 pF load [7, 8]	Clock output limit, CMOS, Automotive	–	–	166	MHz
t_2	Output Duty Cycle [7, 9]	Duty cycle for outputs, defined as $t_2 \div t_1$, Fout < 100 MHz, divider ≥ 2, measured at $V_{DD}/2$	45%	50%	55%	
		Duty cycle for outputs, defined as $t_2 \div t_1$, Fout > 100 MHz or divider = 1, measured at $V_{DD}/2$	40%	50%	60%	
t_3	Rising Edge Slew Rate [7]	Output clock rise time, 20% to 80% of V_{DD}	0.75	1.4	–	V/ns
t_4	Falling Edge Slew Rate [7]	Output clock fall time, 80% to 20% of V_{DD}	0.75	1.4	–	V/ns
t_5	Output three-state Timing [7]	Time for output to enter or leave three-state mode after SHUTDOWN/OE switches	–	150	300	ns
t_6	Clock Jitter [7, 10]	Peak-to-peak period jitter, CLK outputs measured at $V_{DD}/2$	–	400	–	ps
t_7	Lock Time [7]	PLL Lock Time from Power up	–	1.0	3	ms

Notes
7. Guaranteed by design, not 100% tested.
8. Guaranteed to meet 20%–80% output thresholds and duty cycle specifications.
9. Reference Output duty cycle depends on XTALIN duty cycle.
10. Jitter varies significantly with configuration. Reference Output jitter depends on XTALIN jitter and edge rate.

Switching Waveforms

Figure 2. All Outputs, Duty Cycle, and Rise/Fall Time

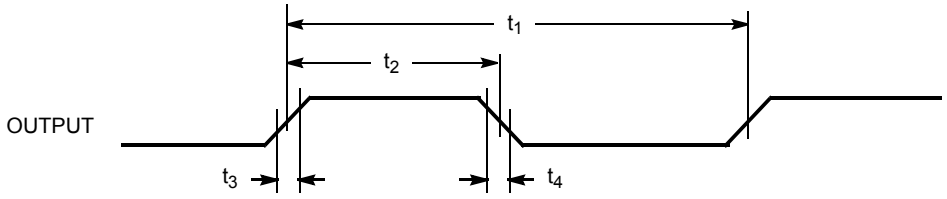


Figure 3. Output Three-State Timing

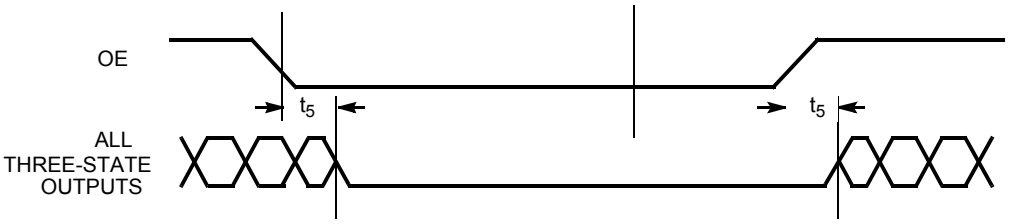


Figure 4. CLK Output Jitter

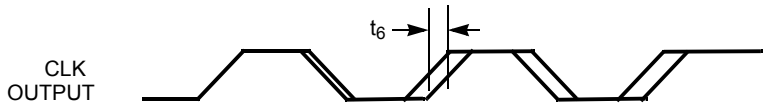
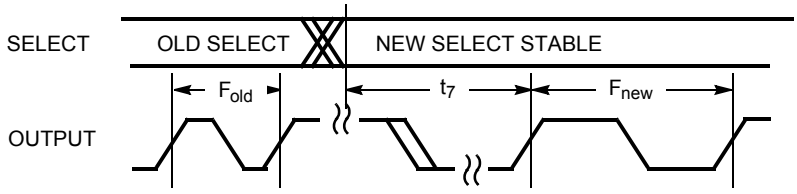
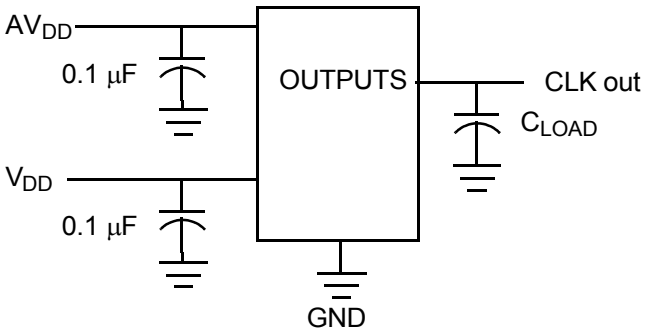


Figure 5. Frequency Change



Test Circuit



Ordering Information

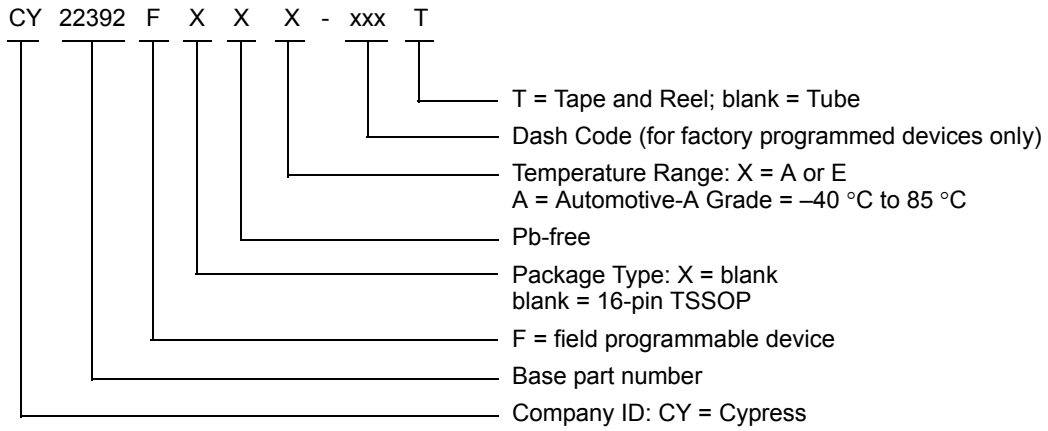
Ordering Code	Package Name	Package Type	Operating Range
Pb-free			
CY22392FXA	ZZ16	16-pin TSSOP	Automotive-A Grade (T_A = –40 °C to 85 °C)
CY22392FXAT	ZZ16	16-pin TSSOP – Tape and Reel	Automotive-A Grade (T_A = –40 °C to 85 °C)
Programmer			
CY3672-USB		FTG Programmer	
CY3698[11]	Only for TSSOP (ZZ16) package	CY22392F, CY22393F CY22394F and CY22395F Adapter for CY3672-USB	

Some product offerings are factory programmed, customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

Possible Configurations

Ordering Code	Package Name	Package Type	Operating Range
Pb-free			
CY22392ZXA-xxx [12]	ZZ16	16-pin TSSOP	Automotive-A Grade (T_A = –40 °C to 85 °C)
CY22392ZXA-xxxT [12]	ZZ16	16-pin TSSOP – Tape and Reel	Automotive-A Grade (T_A = –40 °C to 85 °C)

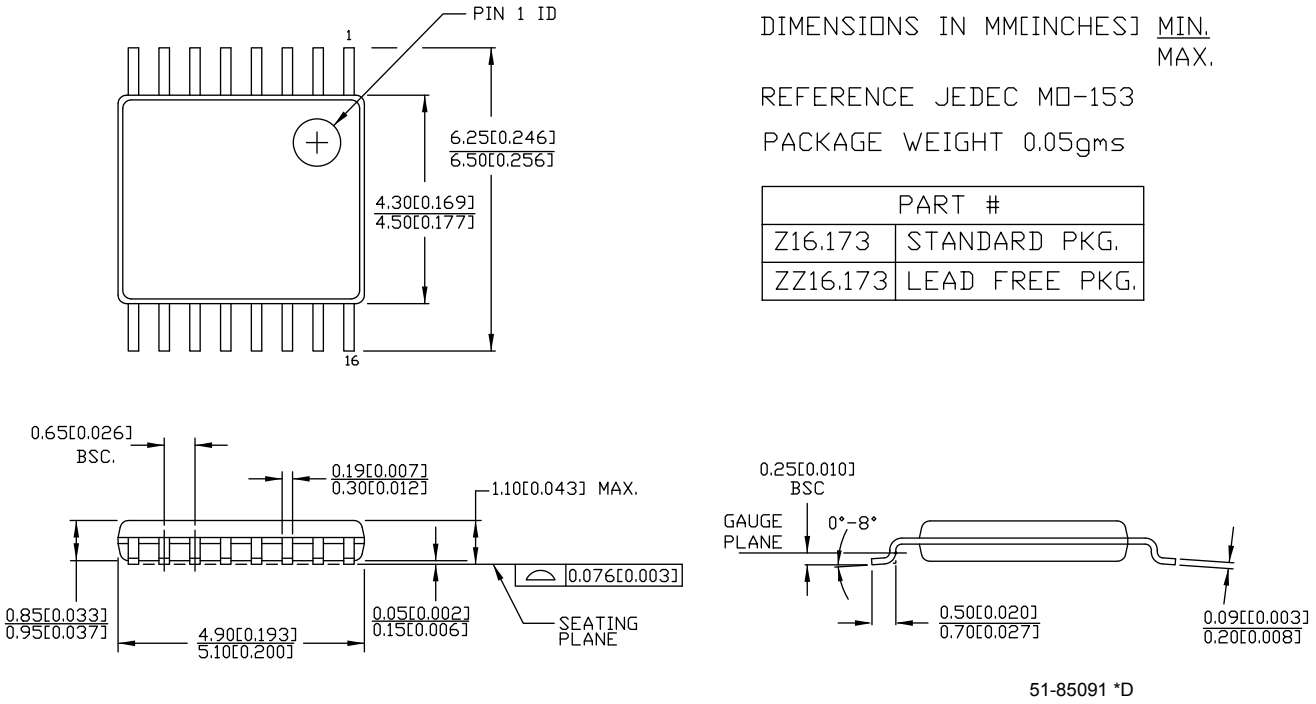
Ordering Code Definitions



Notes
11. Programming of only 16-pin TSSOP package is supported by CY3698.
12. The CY22392ZX are factory programmed configurations. Factory programming is available for high-volume design opportunities of 100 Ku/year or more in production. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Package Diagrams

Figure 6. 16-pin TSSOP 4.40 mm Body Z16.173/ZZ16.173 Package Outline, 51-85091



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EMI	Electromagnetic Interference
FET	Field-Effect Transistor
FTG	Frequency Timing Generator
JEDEC	Joint Electron Devices Engineering Council
LVTTL	Low Voltage Transistor-Transistor Logic
OSC	Oscillator
PCB	Printed Circuit Board
PLL	Phase Locked Loop
TSSOP	Thin Shrink Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µF	microfarad
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY22392 Automotive, Three-PLL General Purpose Flash Programmable Clock Generator Document Number: 001-88434				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4062529	CINM	08/23/2013	New data sheet.
*A	4322006	CINM	04/23/2014	Updated Features: Added Automotive-E grade temperature related information. Updated Device Programming: Added “Programming of the clock device should be done at temperatures < 75 °C.” Updated Maximum Ratings: Added “Data Retention at Tj = 150 °C” as “> 2 years”. Added “Package Power Dissipation (E-Grade)” as “217 mW”. Added “Stresses exceeding absolute maximum conditions may cause permanent damage to the device. These conditions are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this data sheet is not implied. Extended exposure to Absolute Maximum Conditions may affect reliability.” Updated Electrical Characteristics: Added Note 5 and referred the same note in Conditions of I_{OH} and I_{OL} parameters. Updated Conditions of I_{OZ} parameter. Added Note “Profile configuration through CyberClocks (JEDEC file) should be so generated such that for E-Grade, $I_{DDmax} \leq 56$ mA (considering T_{Amax} = 125 °C).” referred the same note in Conditions of I_{DD} parameter. Added Note 6 and referred the same note in Conditions of I_{DD} parameter. Updated Ordering Information: Updated part numbers.
*B	4528309	TAVA	10/08/2014	Changed status from Preliminary to Final. Removed Automotive-E grade temperature related information in all instances across the document. Updated Electrical Characteristics: Removed Note “Profile configuration through CyberClocks (JEDEC file) should be so generated such that for E-Grade, $I_{DDmax} \leq 56$ mA (considering T_{Amax} = 125 °C).” and its reference in I_{DD} parameter. Updated Ordering Information: Updated part numbers. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support