MP3212

1.3A, 1MHz Step-up Regulator with Integrated Input Disconnect Switch

DESCRIPTION

The MP3212 is a high efficiency, fixed frequency, current-mode boost converter with input disconnect, inrush current limiting, internal soft-start and compensation.

The 1MHz switching frequency allows for smaller external components producing a compact solution for a wide range of load currents. The input disconnect feature provides complete isolation from output to input when the device is in either shutdown mode or fault condition. The internal compensation minimizes the external component count and soft-start limits the current during startup. The MP3212 automatically transitions into pulse-frequency modulation mode to achieve better efficiency at light load. The input voltage range of 2.3V to 5.5V can generate 28V at up to 100mA.

The MP3212 includes under-voltage lockout, current limit, over voltage protection and thermal shutdown. In addition to cycle by cycle current limit at power switch, the average current is also monitored at disconnect switch to prevent damage in the event of output overload.

The MP3212 is offered in a compact 10-pin QFN (3x3mm) package.

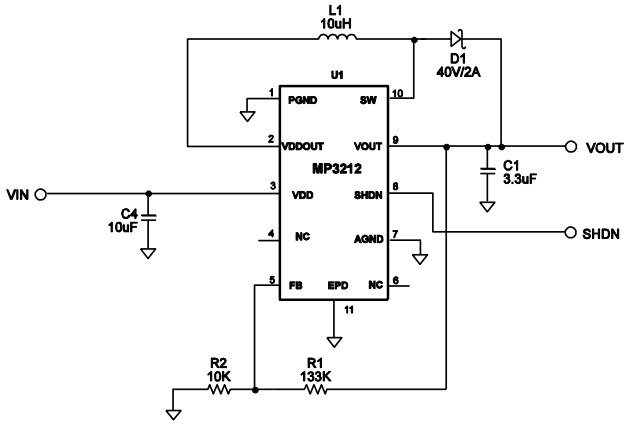
FEATURES

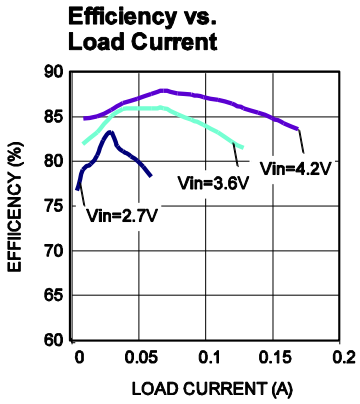
- Up to 88% Efficiency
- 2.3V to 5.5V Input Voltage
- Up to 28V Output
- 1 MHz Fixed Switching Frequency
- Integrated Power MOSFET
- Integrated Input Disconnect Switch
- Zero Current Shutdown Mode
- Internal Soft-Start
- Internal Compensation
- Automatic Pulse Frequency Modulation Mode at Light Load
- Inrush Current Limiting
- 1.3A Typical Switch Current Limit
- Under voltage lockout
- Over Voltage Protection
- Thermal Shutdown
- 10-Pin QFN (3x3mm) Package

APPLICATIONS

- Low Noise Power Supply
- Wimax RF Amp Power Supply
- GPRS/GSM RF Amp Power Supply

TYPICAL APPLICATION



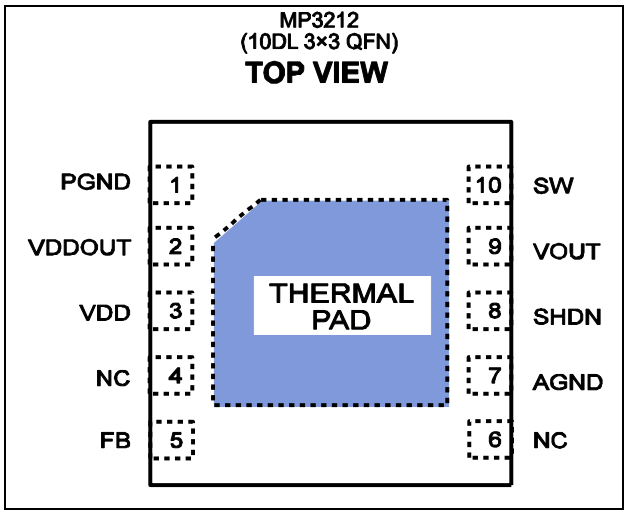


ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP3212DQ	QFN10 (3mm x 3mm)	7F	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP3212DQ–Z). For RoHS Compliant Packaging, add suffix –LF (e.g. MP3212DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VDD to GND ..... –0.3V to +6V
VOUT to GND..... –0.3V to +35V
VSW to GND ..... –0.5V to +36V
All Other Pins..... –0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
.....2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN}.....2.3V to 5.5V
Output Voltage V_{OUT} 28Vmax
Operating Temperature ..... –40°C to +85°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN10 (3×3mm) .....50 ..... 12 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 3.6V, V_{GND} = V_{SHDN} = 0V, T_A = 25°C. C_{IN}=10μF, C_{OUT}=3.3μF, L=10μH, R1=10kΩ, R2=133kΩ, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Operating Voltage (1)	V_{DD}		2.3		5.5	V
Under Voltage Lockout High Threshold	$V_{UVLO,HI}$	V_{DD} rising		2.2	2.3	V
Under Voltage Lockout Low Threshold	$V_{UVLO,LO}$	V_{DD} falling	1.8	2		V
Shutdown Current	$I_{Q,SHDN}$	V_{SHDN} = V_{DD}			1	μA
Supply Current (PFM)	$I_{Q(PFM)}$	Not switching		180		μA
Supply Current (PWM)	$I_{Q(PWM)}$	Not switching		400		μA
Switching Frequency	F_{SW}		0.85	1	1.15	MHz
Minimum On time	$t_{ON, MIN}$			80		ns
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0V	90			%
SW On-Resistance	$R_{DS (ON)}$	I(SW) = 100mA		0.4		Ω
SW Leakage	I_{SW}	V_{SHDN} = V_{DD}, V_{SW} = 30V		1	5	μA
SW Current Limit	I_{LIM}			1.3		A
Input Disconnect On-Resistance	$R_{DS (ON)\_VDDOUT}$	I_{OUT} = 50mA, t>2.048ms(2) SHDN = 0V		0.2		Ω
Input Disconnect Leakage Current	I_{SW_VDDOUT}	V_{DDOUT} = 0V			1	μA
Soft Inrush Current Source at V_{DDOUT}	I_{SS_VDDOUT}	V_{DD} –V_{DDOUT} = 0.5V, t_{ON} <2.048ms(2)		120		mA
Logic High Voltage	V_{HI}		2			V
Logic Low Voltage	V_{LO}				0.7	V
Pull-up Resistor	R_{UP}	Enabled, Input at GND		1		MΩ
FB Voltage	V_{FB}		1.2	1.23	1.26	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.23V	-0.1		0.1	μA
Leakage Current when Disabled	$I_{LEAKAGE}$	Disabled, Input at GND		1		μA
Thermal Shutdown	T_{SHDN_TH}			150		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			25		°C
Over-voltage Thershold	V_{OV}	FB=GND	31	34		V
Over-current Thershold	I_{OI}	t>2.048ms(2), DC current		1.7		A
Load Regulation	ΔV_{OUT} / ΔI_{OUT}	I_{OUT} = 50mA to 100mA		0.1		%
Line Regulation	ΔV_{OUT} / ΔV_{DD}	V_{DD} = 3.6V to 2.6V, I_{OUT} = 50mA		0.1		%/V

Notes:

1) Minimum supply operating voltage needs to be above 2.5V at -40°C.
2) Timer is around 2ms-4ms.
3) Guaranteed by design, not tested.

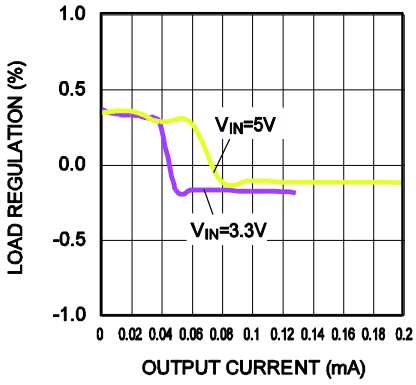
PIN FUNCTIONS

QFN10 Pin #	Name	Description
1	PGND	Power Ground. The ground return for C_{OUT} and internal switch
2	VDDOUT	Input voltage after passing through the input isolation FET
3	VDD	Actual input voltage before the isolation FET
4	NC	No Connect
5	FB	Feedback voltage.
6	NC	No Connect
7	AGND	Analog ground
8	SHDN	Shutdown. Active high
9	VOUT	Output Voltage
10	SW	Switch node.

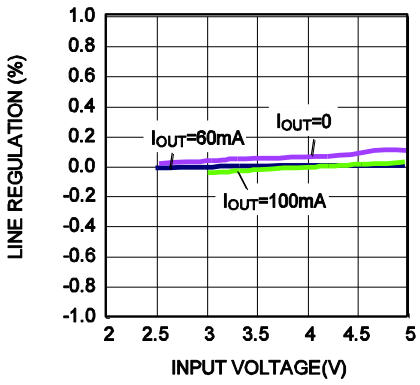
TYPICAL PERFORMANCE CURVES

V_{IN} = 3.3V, V_{OUT} = 18V, T_A = +25ºC, unless otherwise noted.

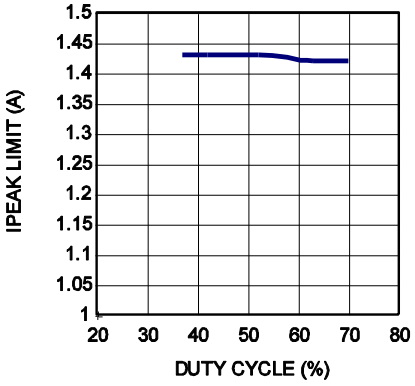
Load Regulation



Line Regulation

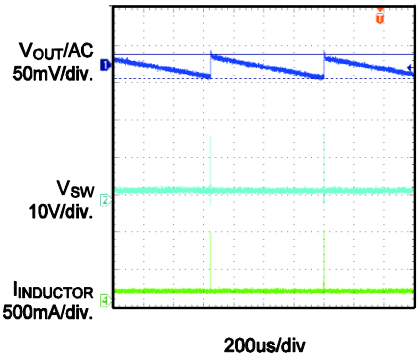


SW peak current limit vs. Duty Cycle



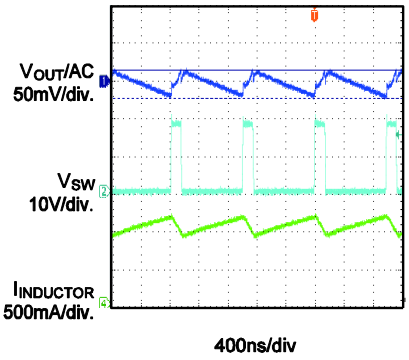
PFM Operation

No Load



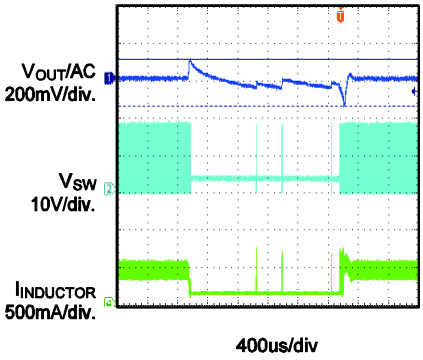
PWM Operation

I_{OUT}=130mA



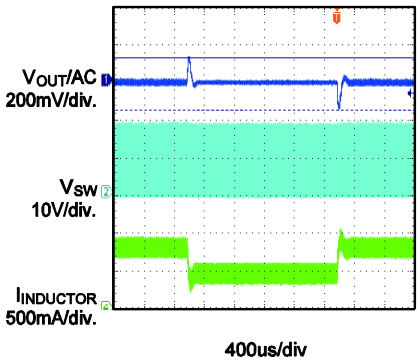
Transient Response

I_{OUT}=0mA-50mA



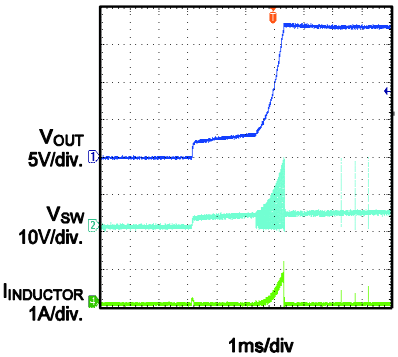
Transient Response

I_{OUT}=50mA-100mA



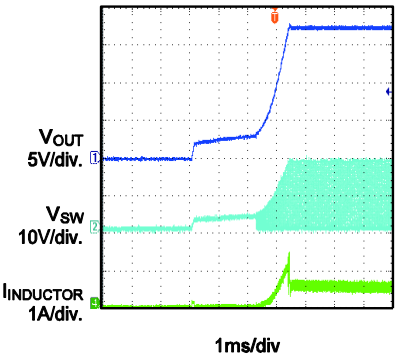
Startup

I_{OUT}=0



Startup

I_{OUT}=100mA

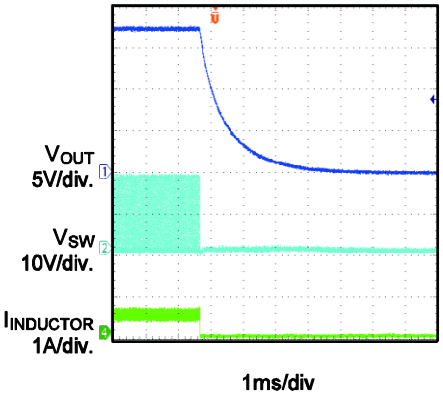


TYPICAL PERFORMANCE CURVES *(continued)*

V_{IN} = 3.3V, V_{OUT} = 18V, T_A = +25ºC, unless otherwise noted.

Shut Down

I_{OUT}=100mA



BLOCK DIAGRAM

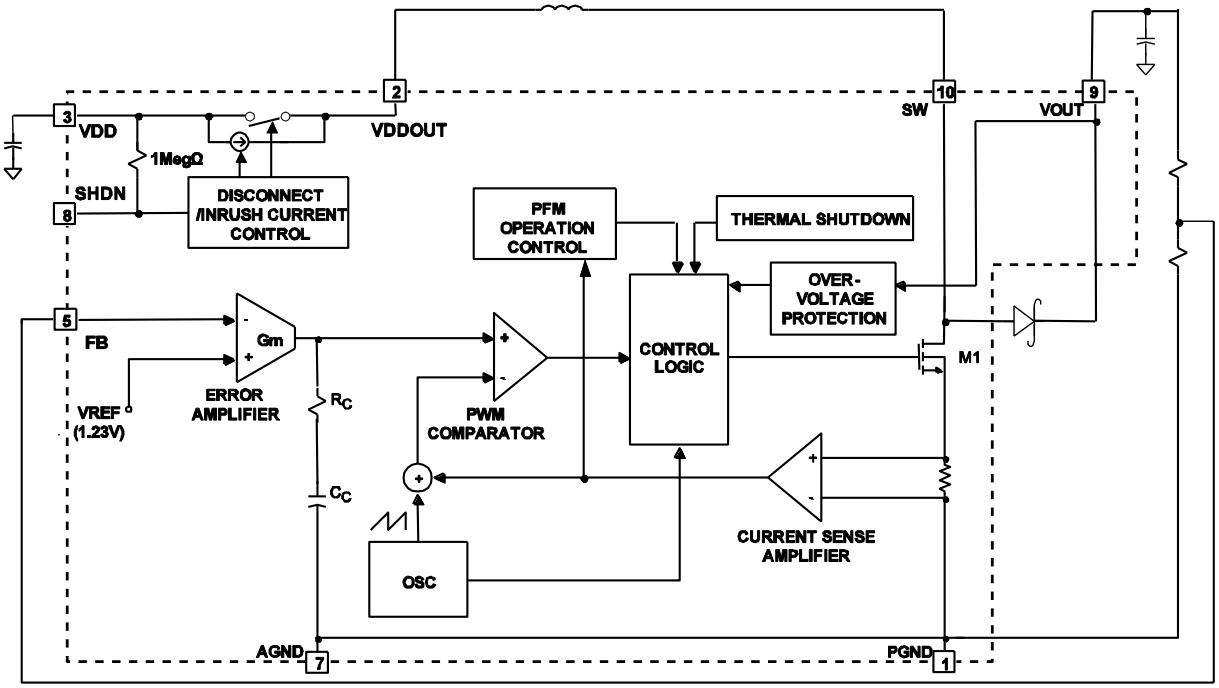


Figure 1—Functional Block Diagram

OPERATION

The MP3212 uses a constant frequency, peak current mode boost regulation architecture to regulate the feedback voltage. The operation of the MP3212 can be understood by referring to the block diagram of Figure 1.

At the beginning of each cycle, the power MOSFET-M1 turns on, to prevent sub-harmonic oscillations at duty cycles greater than 50%, a stabilizing ramp is added to the output of the current sense amplifier. When the output voltage of current sense amplifier equals to the output voltage of error amplifier, the power MOSFET-M1 turns off.

The voltage at the output of the error amplifier is an amplified version of the difference between the 1.23V reference voltage and the feedback voltage. The peak inductor current is corresponded to the error amplifier output. If the feedback voltage starts to drop, the output of error amplifier increases, which results in more current flowing through the power MOSFET-M1 and thus increases the power delivered to the output. The use of current mode control improves transient response.

To prevent the battery from discharging, when MP3212 is disabled, the inductor is automatically disconnected from the input supply.

The MP3212 has internal soft start control and internal loop compensation to save external components.

The MP3212 monitors input under voltage conditions, output over voltage conditions, and over temperature events for input under voltage lockout, output over voltage protection and over temperature protection.

Start-Up Sequence

After SHDN pin is pulled low, or a restart is triggered by the fault condition, MP3212 will go through a start up sequence described as below.

At the beginning of start up, the VDDOUT switch is configured as the current source to regulate the inrush current, and pre-charge the capacitor at Vout. There is 2ms timer to make sure the capacitor at Vout is charged up close to Vin minus a diode drop. However, if Vout is still not charged up after timeout, MP3212 will stay in this mode.

After 2ms timeout, if Vout is charged up close to Vin minus a diode drop, then the VDDOUT switch will be fully turned on and connect the inductor to VDD. MP3212 will enter soft start.

The error amplifier voltage is increased slowly during soft start to prevent overshoot. When VFB approaches the internal band-gap voltage, the MP3212 starts normal operation.

Fault Control

FAULT DESCRIPTION	FAULT CONDITION	FAULT REACTION
Under-voltage at VDD	$V(VDD) < V_{UVLO,LO}$	Disables I/Os and waits until V(VDD) reaches $V_{UVLO,HI}$ on to begin with the start-up sequence
Over-current drawn from VDDOUT	$I(VDDOUT) > I_{OI}$	Disables VDDOUT switch and SW switch and immediately restarts the start-up sequence
Over-voltage at VOUT	$V(VOUT) > V_{OV}$	Disables VDDOUT switch and SW switch and waits until output voltage V(VOUT) drops to V_{OV}- V_{OV_Hys} to restart the start-up sequence
Over Temperature on chip	$Tj > T_{SHDN\_TH}$	Disables VDDOUT switch and SW switch and waits until junction temp drops to T_{SHDN_TH}- T_{SHDN_HYS} to restart the start-up sequence

Maximum Duty Cycle
The maximum duty cycle Dmax will determine the maximum output voltage that the MP3212 can provide. The maximum duty cycle is defined by the minimum off time of the switch.
DMAX = 1 – to_{FF}*Fosc

PFM Mode

During the light load condition, the MP3212 automatically enters pulse frequency modulation (PFM) mode. In PFM mode, most of the internal circuitry is turned off, only keeping alive the active circuitry required to regulate the output voltage.

Isolation From V_{IN} (SHDN=High)
To prevent the battery from discharging the MP3212 is automatically disconnected from the battery when put in shutdown mode. The MP3212 has an internal, low resistance isolation FET that opens when the SHDN pin is pulled high.

Average Current Monitor at the Disconnect Switch
If the average current is above the over current set value VOI, the isolation switch is open, the boost switch is opened, MP3212 then immediately goes into start-up mode.

APPLICATION INFORMATION

Components referenced below apply to Typical Application Circuit on page 1.

Setting the Output Voltage
Set the output voltage by selecting the resistive voltage divider ratio. Use 10kΩ for the low-side resistor R2 of the voltage divider. Determine the high-side resistor R1 by the equation:

$$R1 = \frac{R2 \times (V_{OUT} - V_{FB})}{V_{FB}}$$

where V_{OUT} is the output voltage.

For R2 = 10kΩ and V_{FB} = 1.23V, then

R1 (kΩ) = 8.13 x (V_{OUT} – 1.23) kΩ.

Selecting the Input Capacitor
An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

Use an input capacitor value greater than 4.7μF. The capacitor can be electrolytic, tantalum or ceramic. However since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with RMS current rating greater than the inductor ripple current (see Selecting The Inductor to determine the inductor ripple current).

To ensure stable operation, place the input capacitor as close to the IC as possible. Alternately a smaller high quality ceramic 0.1μF capacitor may be placed closer to the IC with the larger capacitor placed further away. If using this technique, the larger capacitor can be a tantalum or electrolytic type. All ceramic capacitors should be placed close to the MP3212.

Selecting the Output Capacitor
The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristic of the output capacitor also affects the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \approx \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times I_{LOAD}}{C_{OUT} \times f_{SW}}$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, f_{SW} is the switching frequency, and C_{OUT} is the capacitance of the output capacitor.

In the case of tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is calculated as:

$$V_{RIPPLE} \approx \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}}$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the output ripple and load transient requirements of the design. A 3.3µF ceramic capacitor is suitable for most applications.

Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current that results in lower peak inductor current, reducing stress on the internal N-Channel switch. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current.

A 10µH inductor is recommended for most applications. However, a more exact inductance value can be calculated. A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Make sure that the peak inductor current is below 75% of the current limit at the operating duty cycle to prevent loss of regulation due to the current limit. Also make sure that the inductor does not saturate under the worst-case load transient and startup conditions. Calculate the required inductance value by the equation:

$$L = \frac{V_{IN}\times(V_{OUT}-V_{IN})}{V_{OUT}\times f_{SW}\times \Delta I}$$

$$I_{IN(MAX)} = \frac{V_{OUT}\times I_{LOAD(MAX)}}{V_{IN}\times \eta}$$

$$\Delta I = (30\%-50\%) I_{IN(MAX)}$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current, and η is efficiency.

Selecting the Diode

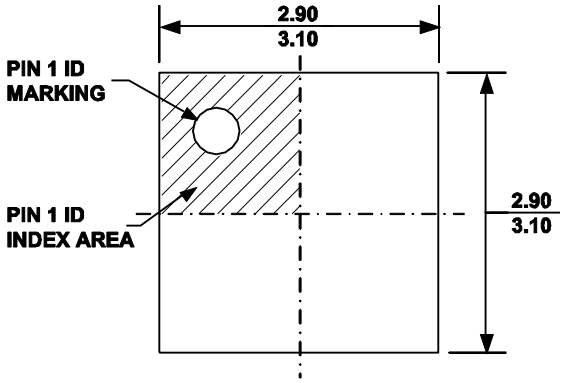
The output rectifier diode supplies current to output when the internal MOSFET is off. To reduce losses due to diode forward voltage and recovery time, use a Schottky diode with the MP3212. The diode should be rated for a reverse voltage greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current.

Layout Consideration

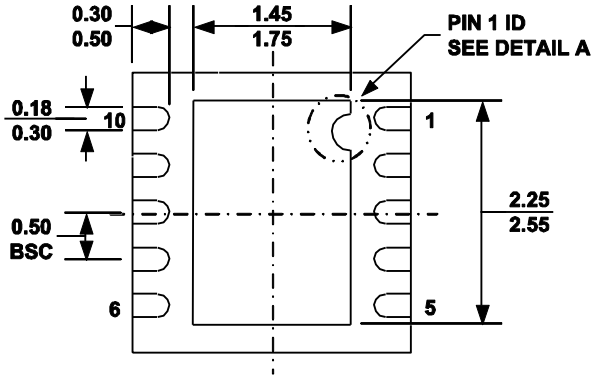
High frequency switching regulators require very careful layout for stable operation and low noise. All components must be placed as close to the IC as possible. Keep the path between the SW pin, output diode, output capacitor and GND pin extremely short for minimal noise and ringing. The input capacitor must be placed close to the IN pin for best decoupling. All feedback components must be kept close to the FB pin to prevent noise injection on the FB pin trace. The ground return of the input and output capacitors should be tied close to the GND pin. See the MP3212 demo board layout for reference.

PACKAGE INFORMATION

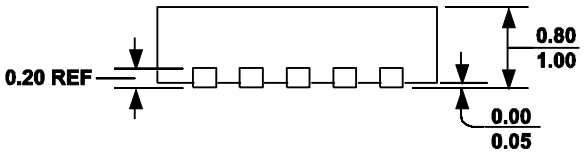
3mm x 3mm QFN10



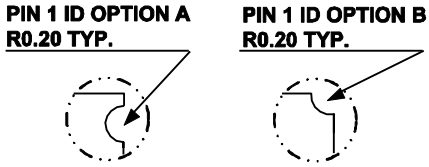
TOP VIEW



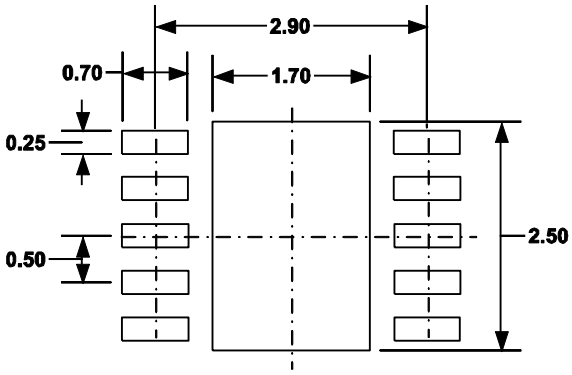
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.