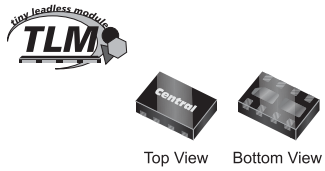
CTLDM7120-M832DS

SURFACE MOUNT
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET



Top View Bottom View

TLM832DS CASE

Central Semiconductor Corp.

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7120-M832DS is an Enhancement-mode Dual N-Channel MOSFET, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. This MOSFET offers Low $r_{DS(ON)}$ and Low Threshold Voltage.

MARKING CODE: CFTS

APPLICATIONS:

- Switching Circuits
- DC-DC Converters
- Battery powered portable devices

FEATURES:

- ESD protection up to 2kV
- Low $r_{DS(ON)}$ (0.25Ω MAX @ V_{GS}=1.5V)
- High current (I_D=1.0A)
- Logic level compatibility

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	8.0	V
Continuous Drain Current (Steady State)	I_D	1.0	A
Maximum Pulsed Drain Current, tp=10μs	I_{DM}	4.0	A
Power Dissipation (Note 1)	P_D	1.65	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	76	°C/W

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=8.0V, V_{DS}=0			10	μA
I_{DSS}	V_{DS}=20V, V_{GS}=0			10	μA
BV_{DSS}	V_{GS}=0, I_D=250μA	20			V
$V_{GS(th)}$	V_{DS}=10V, I_D=1.0mA	0.5		1.2	V
V_{SD}	V_{GS}=0, I_S=1.0A			1.1	V
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=500mA		0.075	0.10	Ω
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=500mA		0.10	0.14	Ω
$r_{DS(ON)}$	V_{GS}=1.5V, I_D=100mA		0.17	0.25	Ω
$Q_{g(tot)}$	V_{DS}=10V, V_{GS}=4.5V, I_D=1.0A		2.4		nC
Q_{gs}	V_{DS}=10V, V_{GS}=4.5V, I_D=1.0A		0.25		nC
Q_{gd}	V_{DS}=10V, V_{GS}=4.5V, I_D=1.0A		0.65		nC
g_{FS}	V_{DS}=10V, I_D=500mA		4.2		S
C_{rss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		45		pF
C_{iss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		220		pF
C_{oss}	V_{DS}=10V, V_{GS}=0, f=1.0MHz		120		pF
t_{on}	V_{DD}=10V, V_{GS}=5.0V, I_D=500mA		25		ns
t_{off}	V_{DD}=10V, V_{GS}=5.0V, I_D=500mA		140		ns

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 54mm^2

R0 (2-March 2012)

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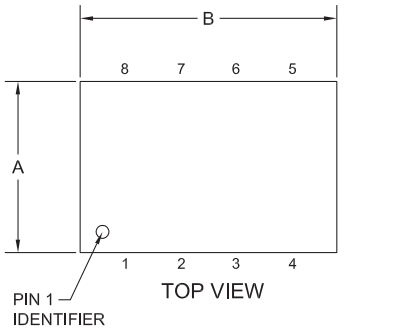
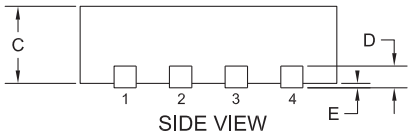
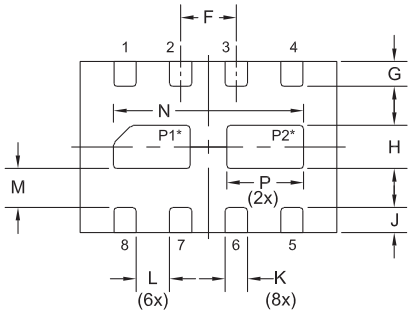
TLM832DS CASE - MECHANICAL OUTLINE





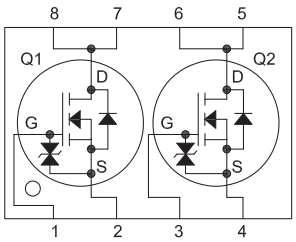


* Exposed pad P1 common to pins 7 and 8
Exposed pad P2 common to pins 5 and 6

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.077	0.081	1.95	2.05
B	0.116	0.120	2.95	3.05
C	0.031	0.039	0.80	1.00
D	0.006	0.010	0.16	0.25
E	0.000	0.002	0.00	0.05
F	0.026		0.65	
G	0.008	0.016	0.19	0.40
H	0.014	0.024	0.35	0.61
J	0.008	0.016	0.19	0.40
K	0.008	0.012	0.21	0.31
L	0.013	0.017	0.34	0.44
M	0.006	–	0.15	–
N	0.087		2.22	
P	0.029	0.039	0.74	1.00

TLM832DS (REV:R1)

PIN CONFIGURATION



LEAD CODE:

1) Gate Q1
2) Source Q1
3) Gate Q2
4) Source Q2
5) Drain Q2
6) Drain Q2
7) Drain Q1
8) Drain Q1

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